

TGD N-Channel Enhancement Mode Power MOSFET

Description

The TGD85H21 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in automotive applications and a wide variety of other applications.

General Features

- $V_{DSS} = 85V, I_D = 210A$ (Note5)
- $R_{DS(ON)} < 3.8m\Omega @ V_{GS} = 10V$

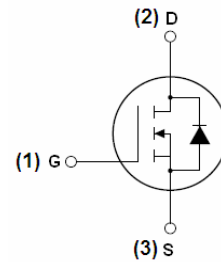
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

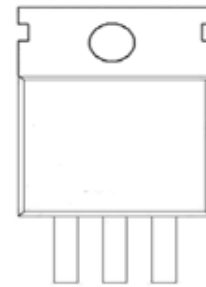
- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

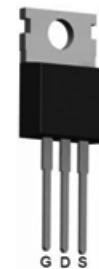
100% ΔV_{ds} TESTED!



Schematic diagram



pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
85H21	85H21	TO-220	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	85	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	210 (Note5)	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D (100^\circ C)$	150	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/ $^\circ C$



Single pulse avalanche energy ^(Note 3)	E_{AS}	2200	mJ
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 1)	$R_{\theta JC}$	0.48	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

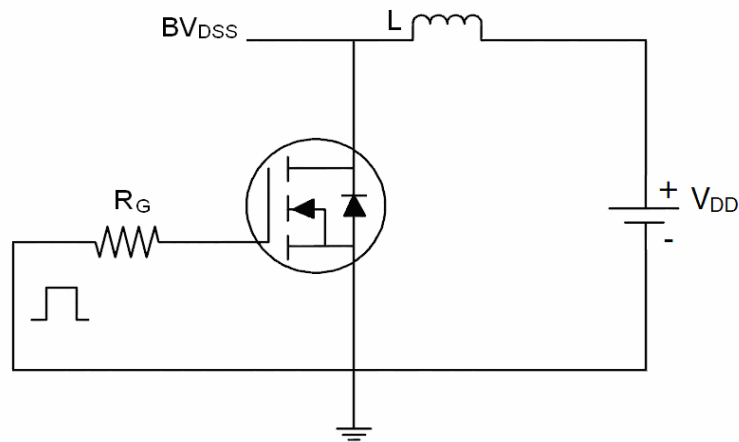
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	85	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=85V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	3.2	3.8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=20A$	35	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	11000	-	PF
Output Capacitance	C_{oss}		-	914	-	PF
Reverse Transfer Capacitance	C_{riss}		-	695	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=38V, I_D=40A$ $V_{GS}=10V, R_{GEN}=1.2\Omega$ ^(Note2)	-	23	-	nS
Turn-on Rise Time	t_r		-	190	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	130	-	nS
Turn-Off Fall Time	t_f		-	120	-	nS
Total Gate Charge	Q_g	$V_{DS}=60V, I_D=40A,$ $V_{GS}=10V$ ^(Note2)	-	250	-	nC
Gate-Source Charge	Q_{gs}		-	48	-	nC
Gate-Drain Charge	Q_{gd}		-	98	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 40A$	-	63	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ ^(Note2)	-	98	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

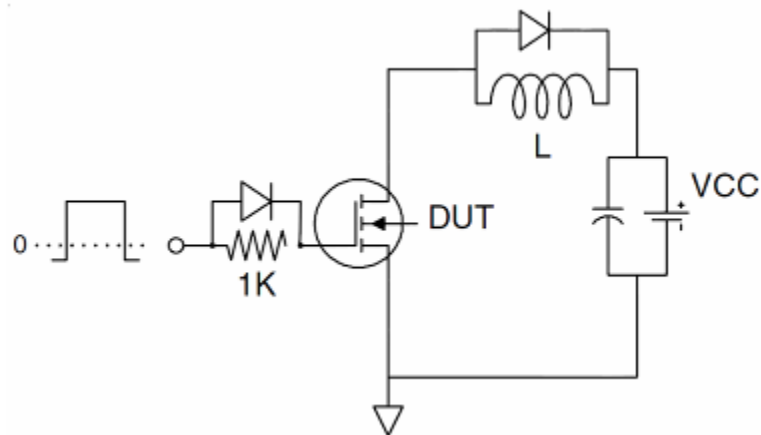
1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 400\mu s$, Duty Cycle $\leq 2\%$.
3. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=42.5V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega, I_{AS}=37A$
4. $ISD \leq 125A, di/dt \leq 260A/\mu s, V_{DD} \leq V(BR)_{DSS}, T_J \leq 175^\circ\text{C}$
5. Package limitation current is 190A.

Test Circuit

1) E_{AS} test Circuit

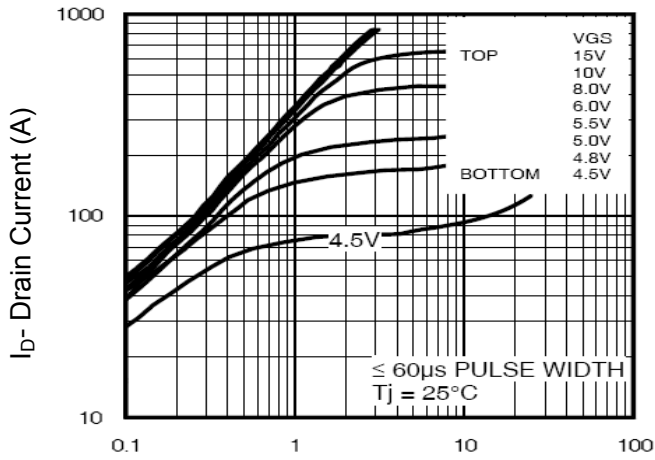


2) Gate charge test Circuit

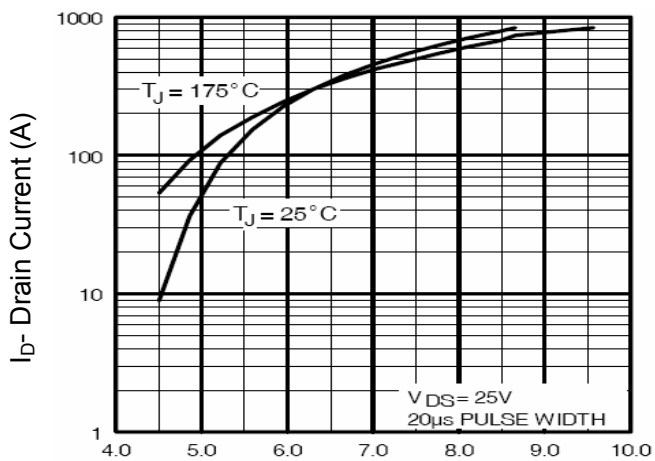


3) Switch Time Test Circuit

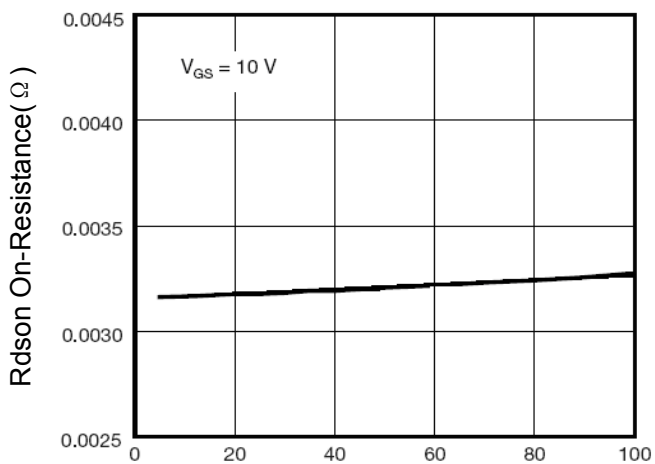
Typical Electrical and Thermal Characteristics



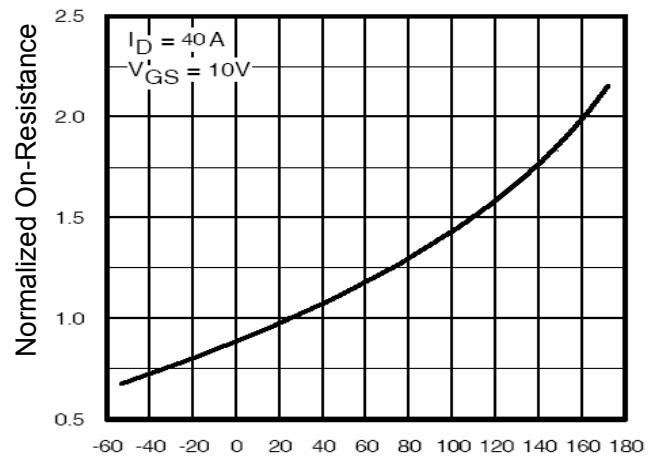
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



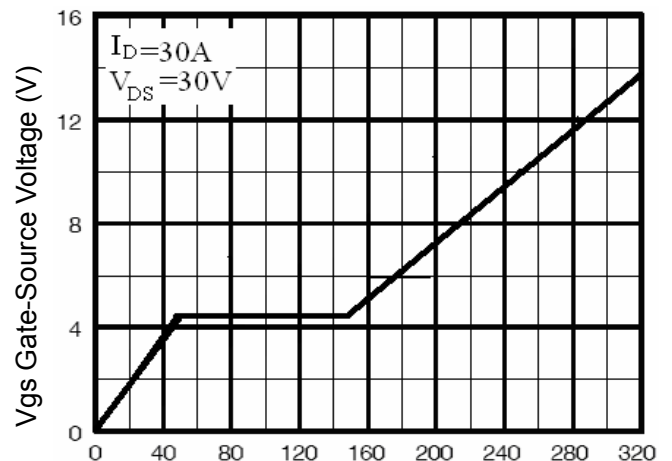
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



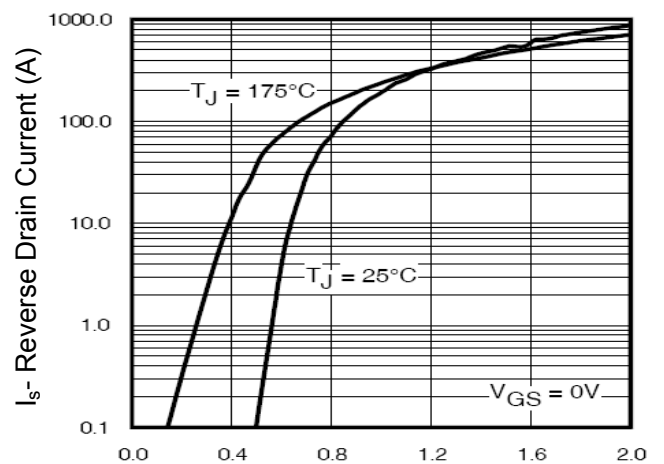
Id- Drain Current (A)
Figure 3 Rdson- Drain Current



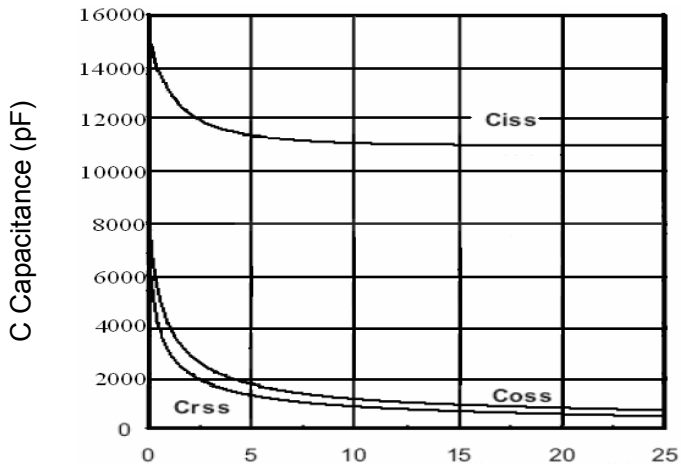
Tj-Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



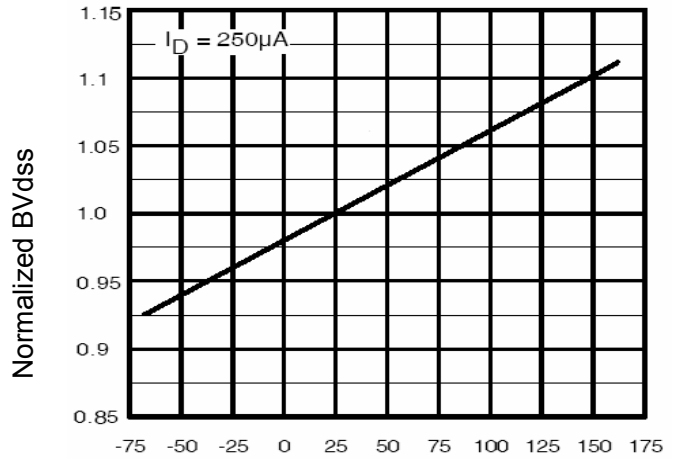
Qg Gate Charge (nC)
Figure 5 Gate Charge



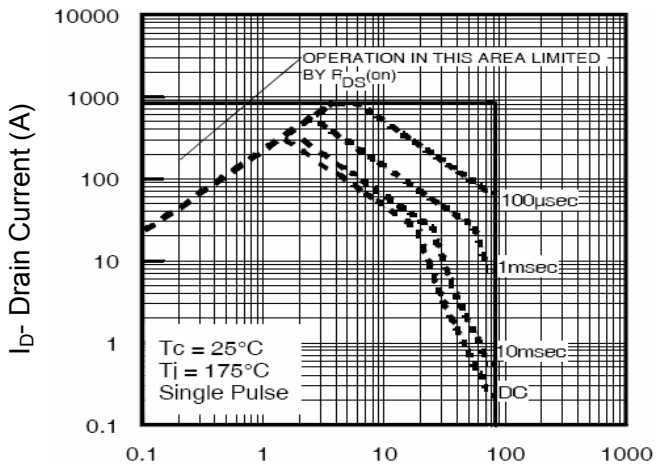
Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



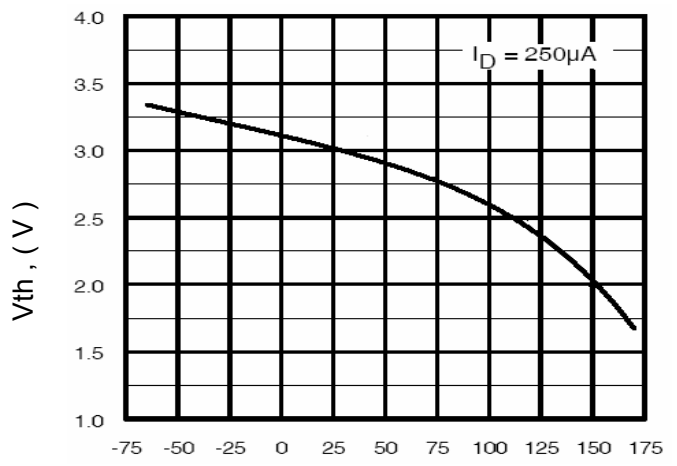
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature

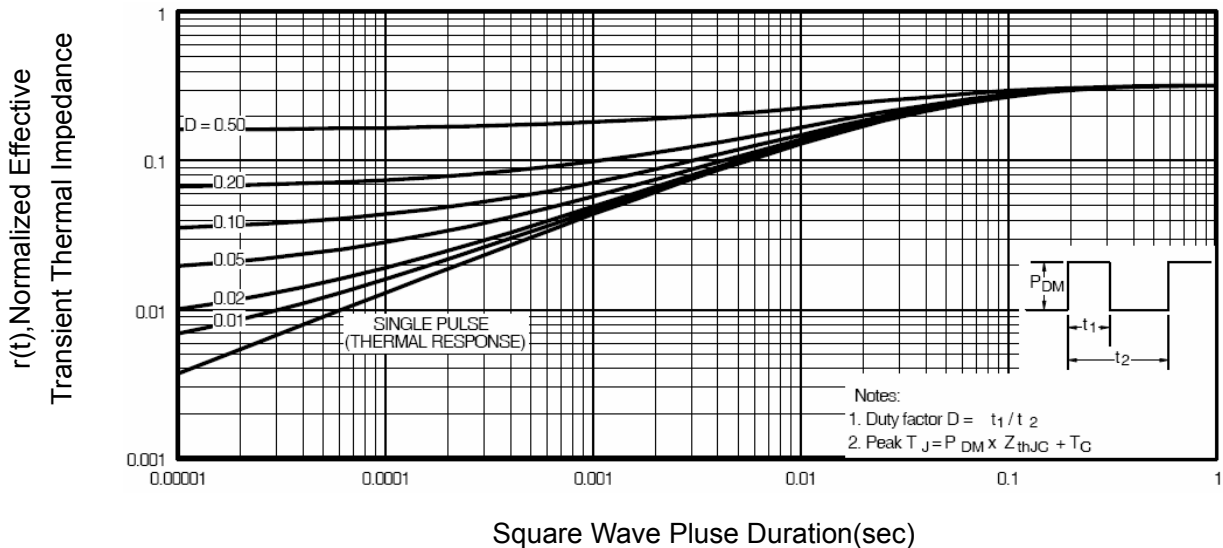
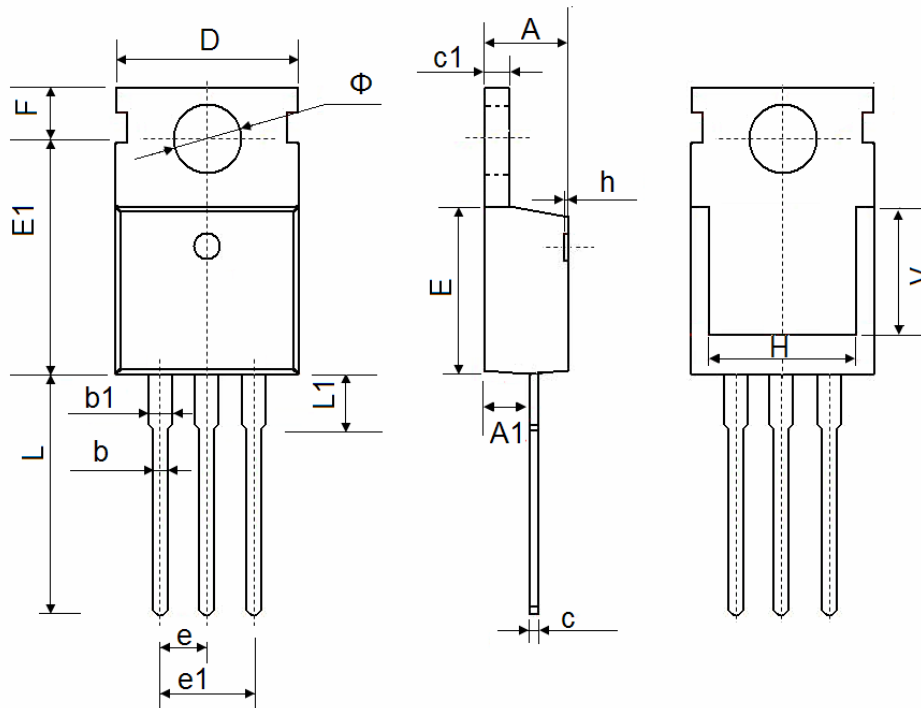


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150