

TGD N-Channel Enhancement Mode Power MOSFET

**Description**

The TGD75H21T uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

**General Features**

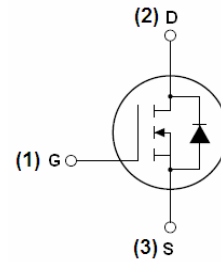
- $V_{DSS} = 75V, I_D = 210A$   
 $R_{DS(ON)} < 4m\Omega @ V_{GS} = 10V$
- Good stability and uniformity with high  $E_{AS}$
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

**Application**

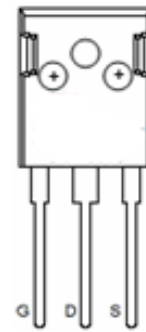
- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

**100% UIS TESTED!**

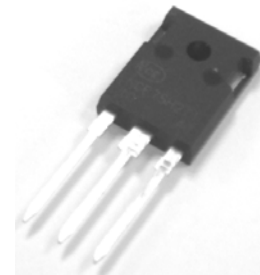
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



pin assignment



TO-247 top view

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD75H21T	TGD75H21T	TO-247	-	-	-

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DSS}$	75	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	210	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	150	A
Pulsed Drain Current	$I_{DM}$	840	A
Maximum Power Dissipation	$P_D$	330	W
Derating factor		2.2	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 4)</sup>	$E_{AS}$	2200	mJ



Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	°C
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**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 1)</sup>	$R_{\theta JC}$	0.455	°C/W
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**Electrical Characteristics (TA=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
<b>Off Characteristics</b>							
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	75			V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=75V, V_{GS}=0V$			1	μA	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			±200	nA	
<b>On Characteristics</b>							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$		25°C	2.9	4	mΩ
				125°C	4.7	6.5	mΩ
Forward Transconductance	$g_{FS}$	$V_{DS}=25V, I_D=40A$	100	165		S	
<b>Dynamic Characteristics</b>							
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$		11000		PF	
Output Capacitance	$C_{oss}$			914		PF	
Reverse Transfer Capacitance	$C_{rss}$			695		PF	
<b>Switching Characteristics</b>							
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		23		nS	
Turn-on Rise Time	$t_r$			190		nS	
Turn-Off Delay Time	$t_{d(off)}$			130		nS	
Turn-Off Fall Time	$t_f$			120		nS	
Total Gate Charge	$Q_g$	$I_D=30A, V_{DD}=30V, V_{GS}=10V$	-	250		nC	
Gate-Source Charge	$Q_{gs}$			48		nC	
Gate-Drain Charge	$Q_{gd}$			98		nC	
<b>Drain-Source Diode Characteristics</b>							
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=40A$			1.2	V	
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C, I_F = 40A$ $di/dt = 100A/\mu s^{(Note2)}$		48		nS	
Reverse Recovery Charge	$Q_{rr}$			78		nC	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)					

**Notes:**

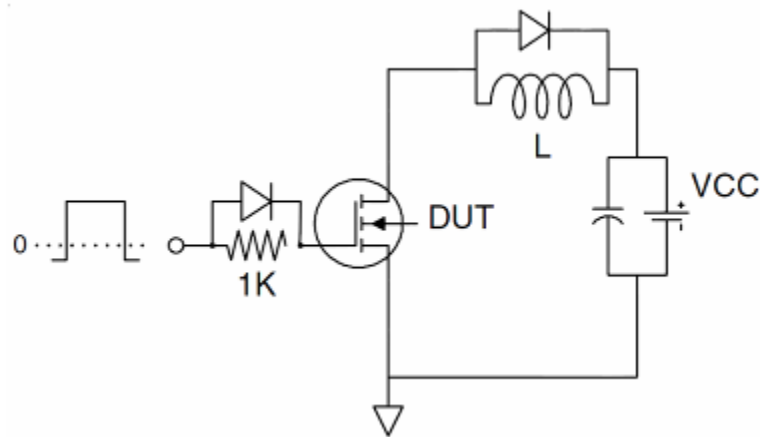
- Surface Mounted on FR4 Board,  $t \leq 10$  sec.
- Pulse Test: Pulse Width  $\leq 400\mu s$ , Duty Cycle  $\leq 2\%$ .
- EAS condition:  $T_J=25^\circ C, V_{DD}=37.5V, V_G=10V, L=0.5mH, R_G=25\Omega, I_{AS}=37A$

**Test circuit**

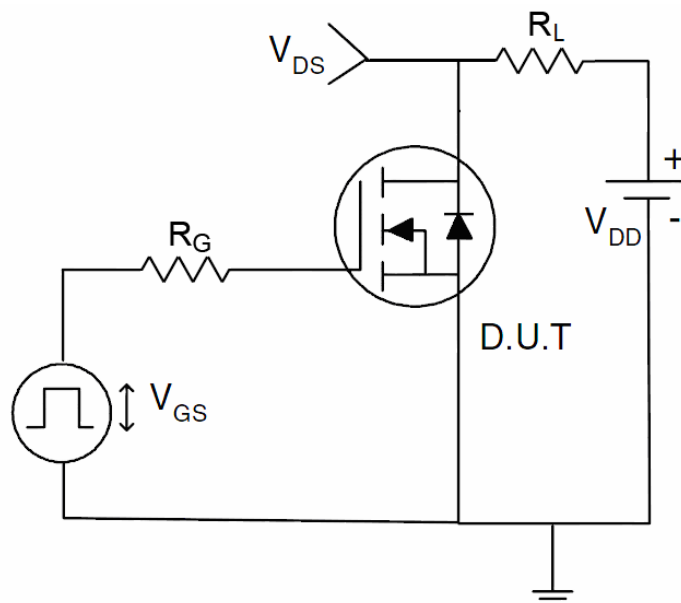
**1) E<sub>AS</sub> test Circuit**



**2) Gate charge test Circuit**



**3) Switch Time Test Circuit**





Typical Electrical and Thermal Characteristics

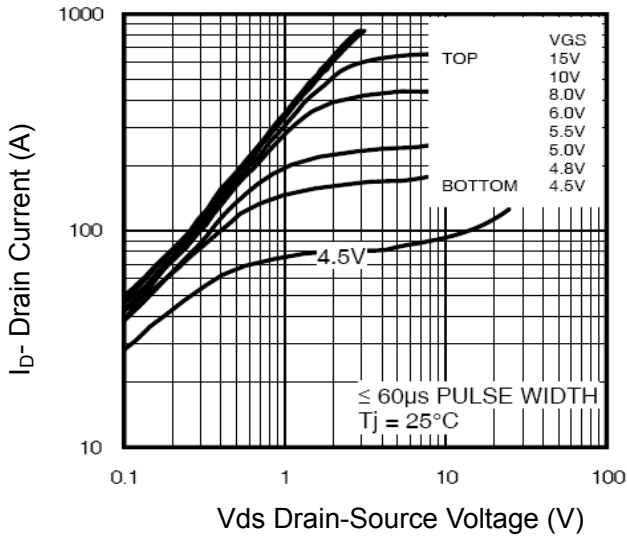


Figure 1 Output Characteristics

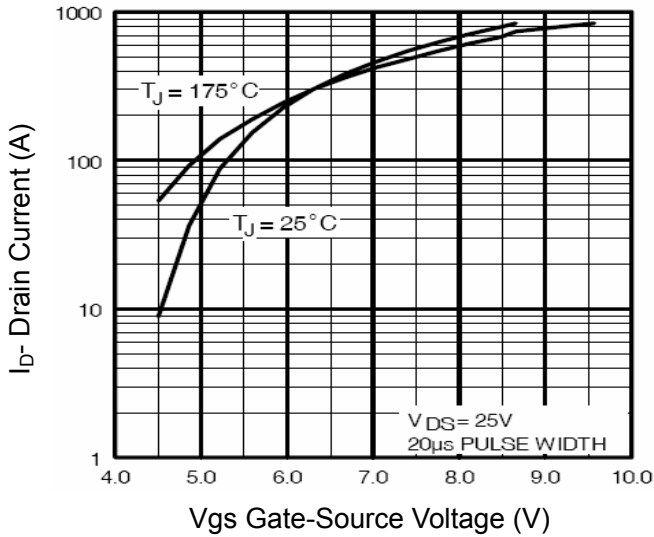


Figure 2 Transfer Characteristics

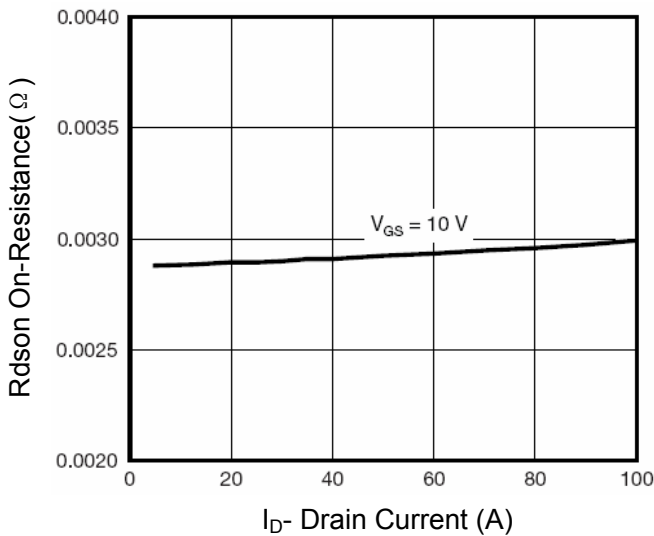


Figure 3 Rdson- Drain Current

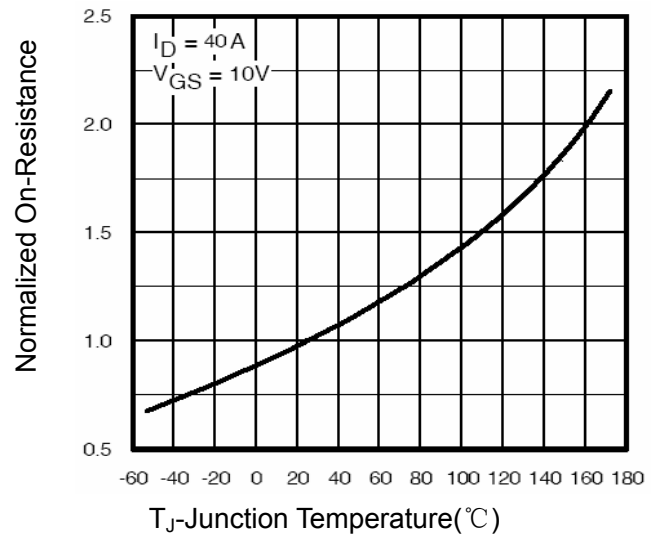


Figure 4 Rdson-Junction Temperature

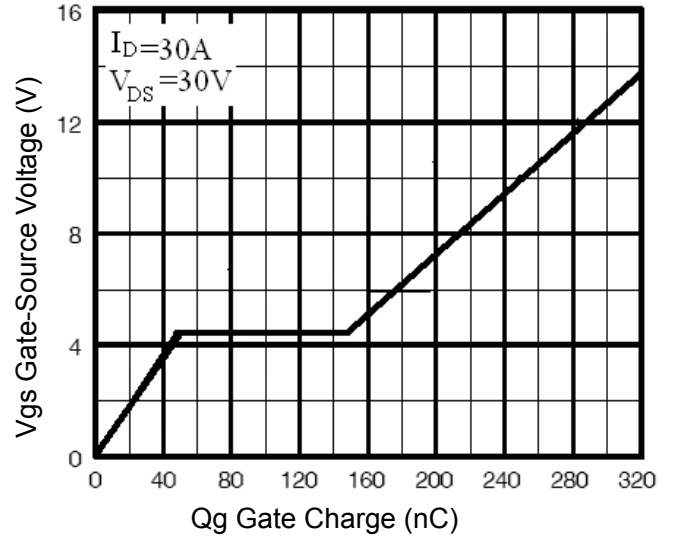


Figure 5 Gate Charge

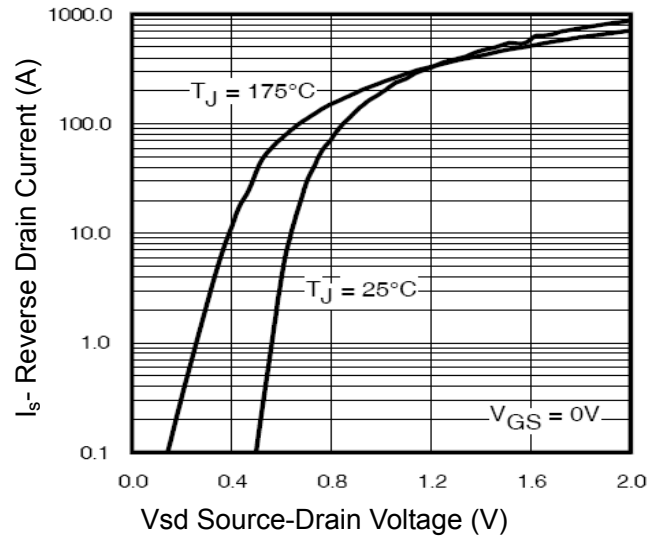


Figure 6 Source- Drain Diode Forward

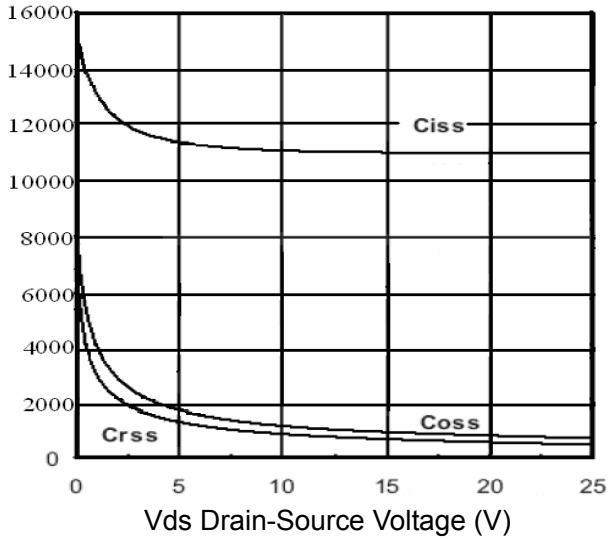


Figure 7 Capacitance vs Vds

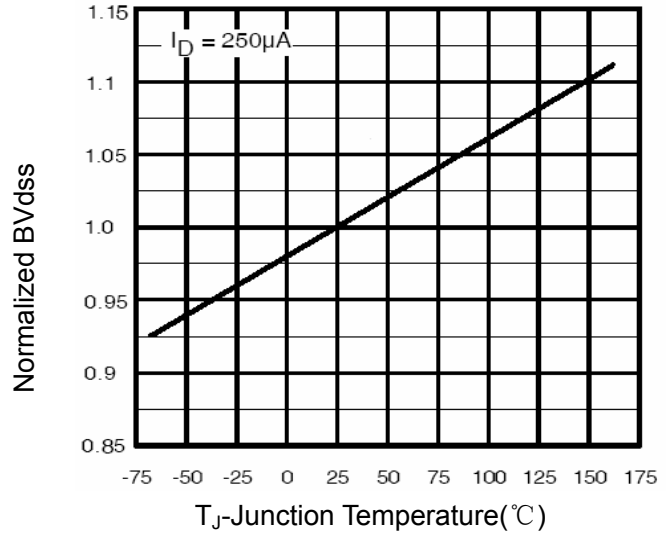


Figure 9 BV<sub>DSS</sub> vs Junction Temperature

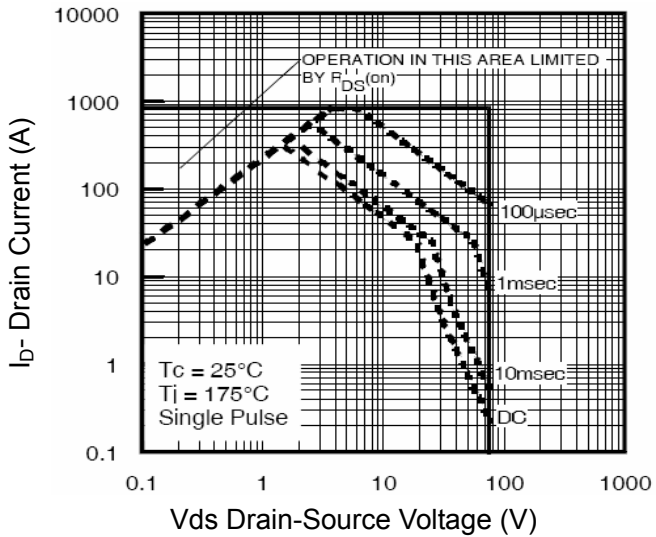


Figure 8 Safe Operation Area

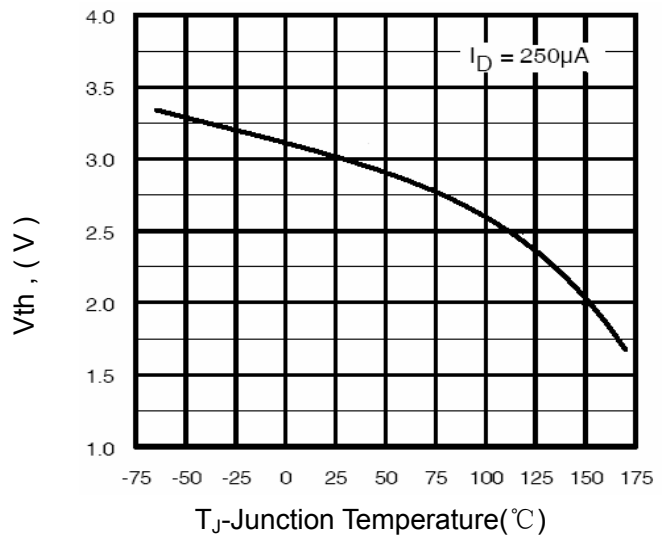


Figure 10 V<sub>GS(th)</sub> vs Junction Temperature

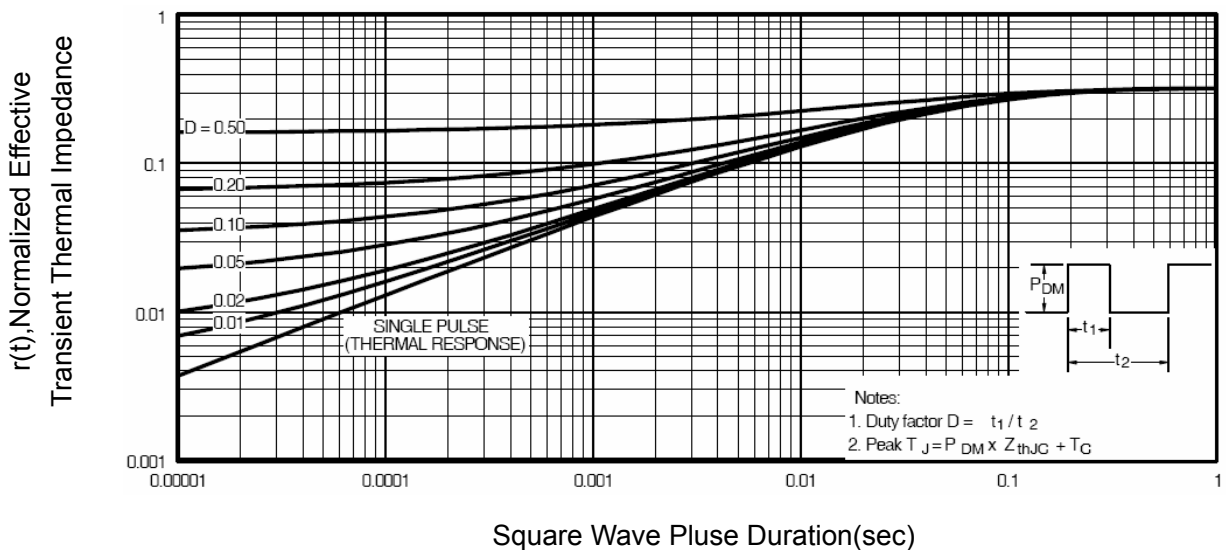
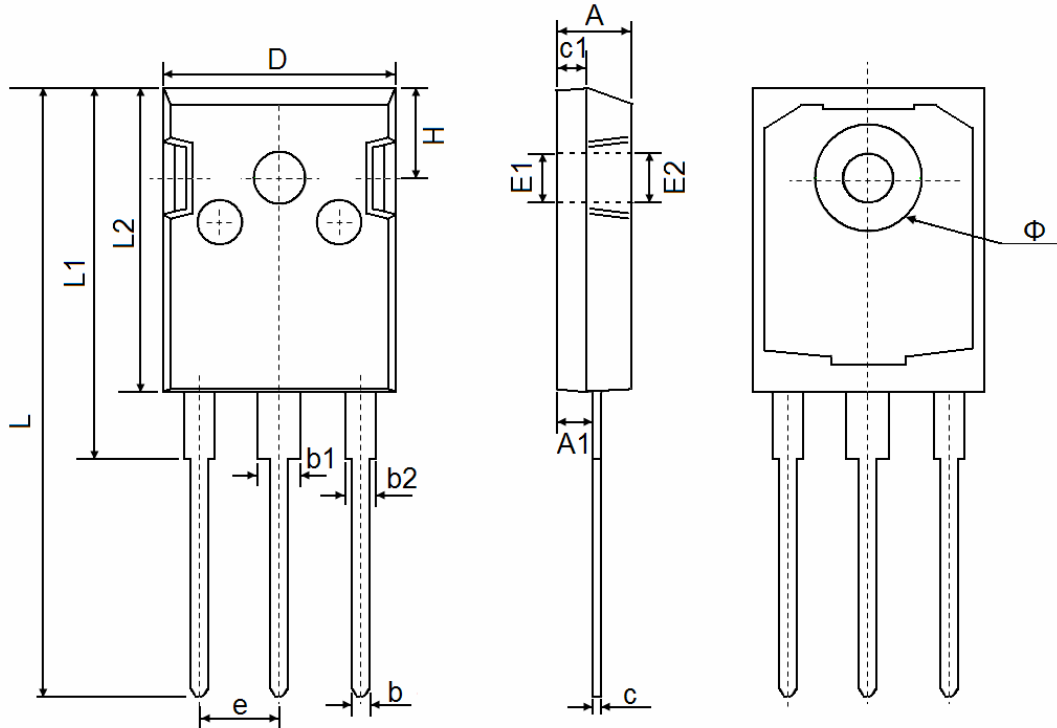


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-247 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	