



## TGD N-Channel Enhancement Mode Power MOSFET

### Description

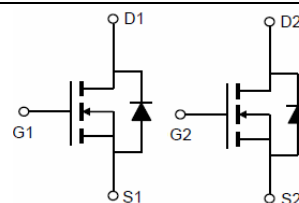
The TGD6005AS uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

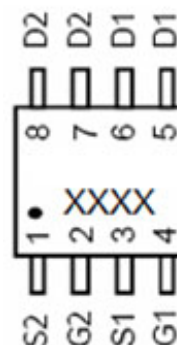
- $V_{DS}=60V, I_D=5A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=10V$  (Typ.26m $\Omega$ )  
 $R_{DS(ON)} < 45m\Omega @ V_{GS}=4.5V$  (Typ.32m $\Omega$ )
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



pin assignment



SOP-8 top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD6005AS	TGD6005AS	SOP-8	Ø330mm	12mm	2500 units

### Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	5	A
Drain Current-Continuous( $T_C=100^{\circ}C$ )	$I_D(100^{\circ}C)$	3.5	A
Pulsed Drain Current	$I_{DM}$	24	A
Maximum Power Dissipation	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	62.5	$^{\circ}C/W$
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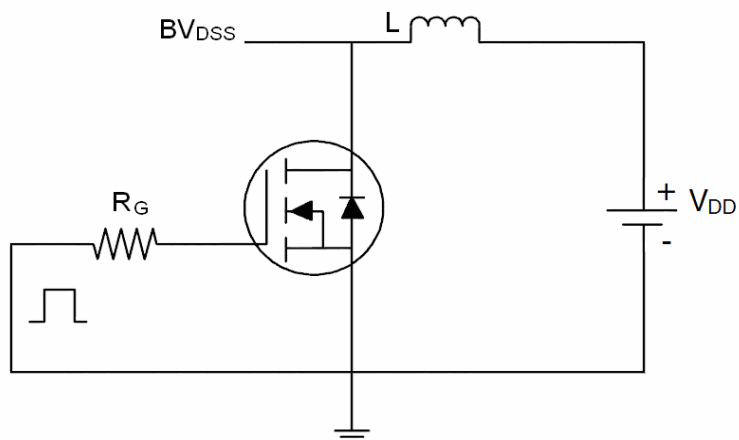
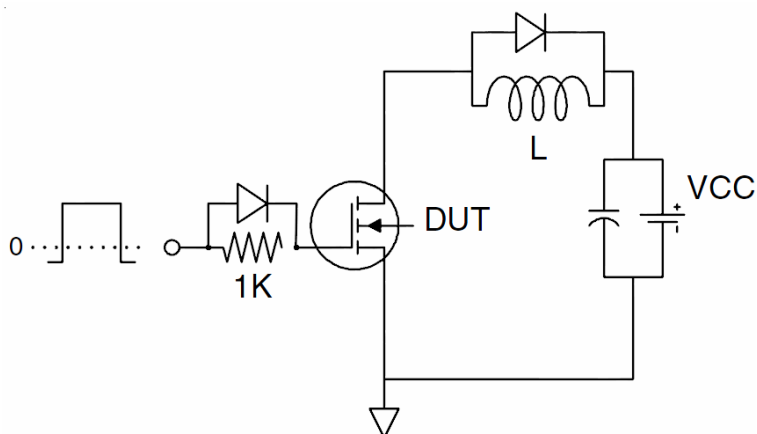
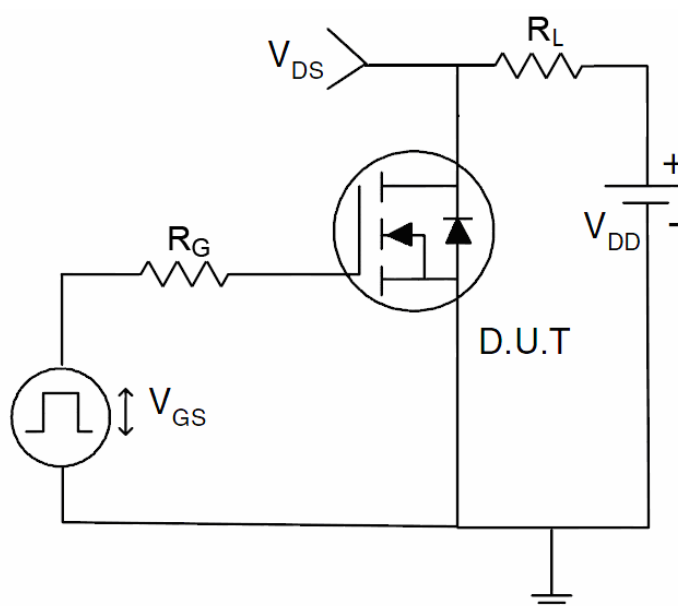


Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

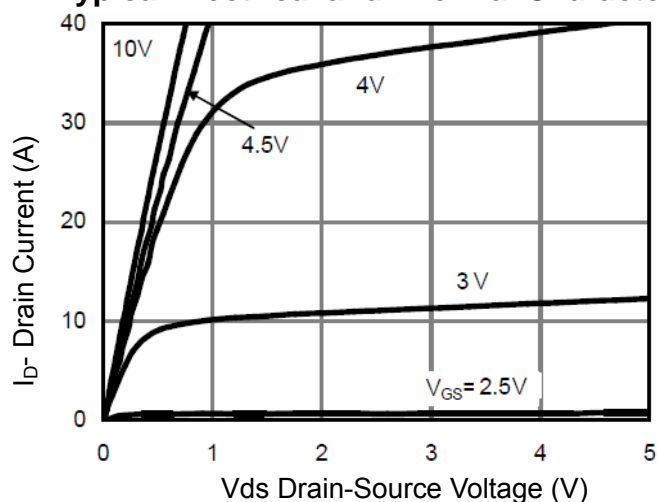
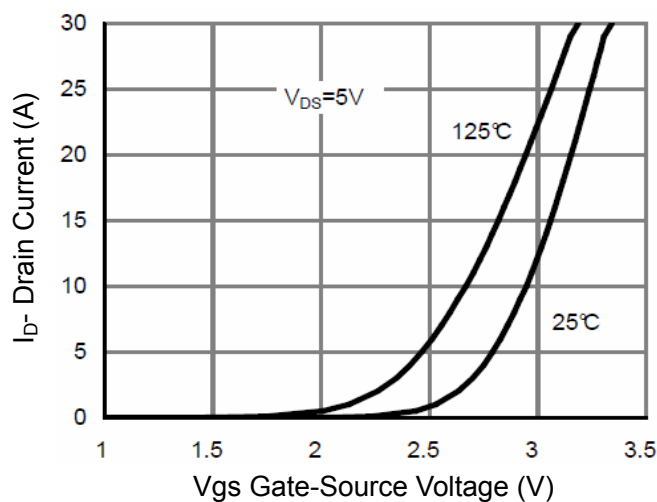
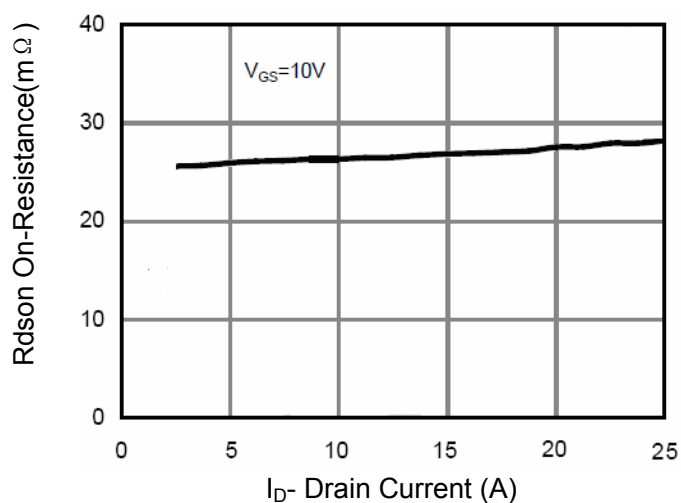
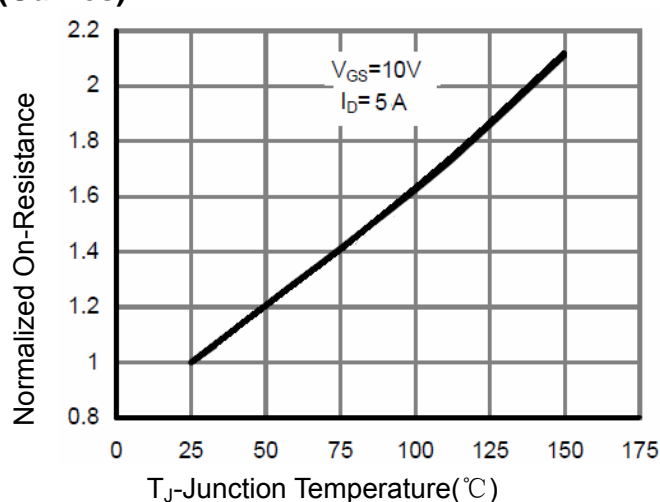
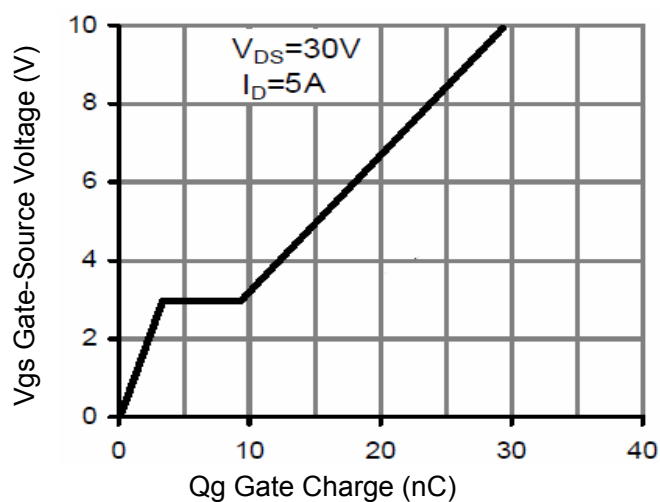
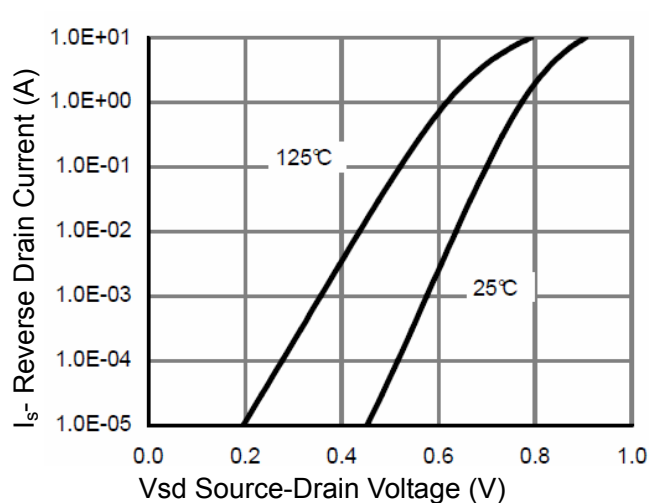
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$	-	26	35	m $\Omega$
	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=5A$	-	32	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=5A$	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	$C_{ISS}$	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	979	-	PF
Output Capacitance	$C_{OSS}$		-	120	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	100	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=6.7\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	5.2	-	nS
Turn-on Rise Time	$t_r$		-	3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	nS
Turn-Off Fall Time	$t_f$		-	2.5	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=30V, I_D=5A,$ $V_{GS}=10V$	-	22		nC
Gate-Source Charge	$Q_{gs}$		-	3.3		nC
Gate-Drain Charge	$Q_{gd}$		-	5.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=5A$	-		1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	5	A
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=30V$ ,  $V_G=10V$ ,  $L=0.5\text{mH}$ ,  $R_g=25\Omega$

**Test Circuit**
**1)  $E_{AS}$  test Circuit**

**2) Gate charge test Circuit**

**3) Switch Time Test Circuit**


### Typical Electrical and Thermal Characteristics (Curves)


**Figure 1 Output Characteristics**

**Figure 2 Transfer Characteristics**

**Figure 3 Rdson- Drain Current**

**Figure 4 Rdson-Junction Temperature**

**Figure 5 Gate Charge**

**Figure 6 Source- Drain Diode Forward**

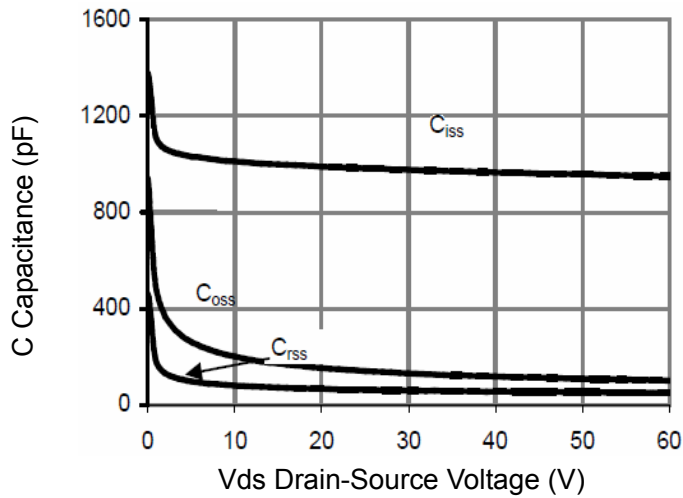


Figure 7 Capacitance vs Vds

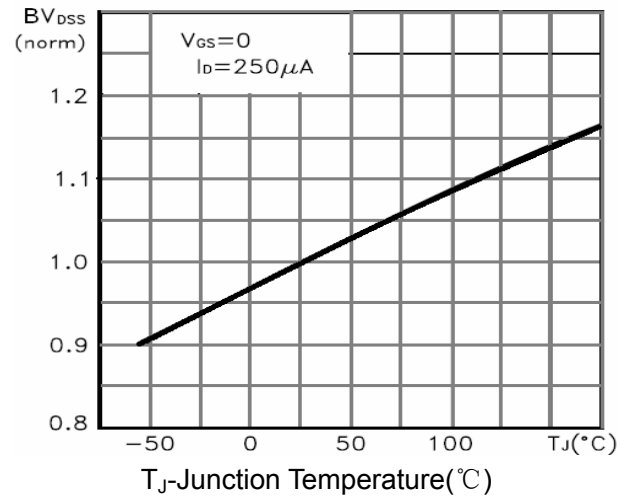
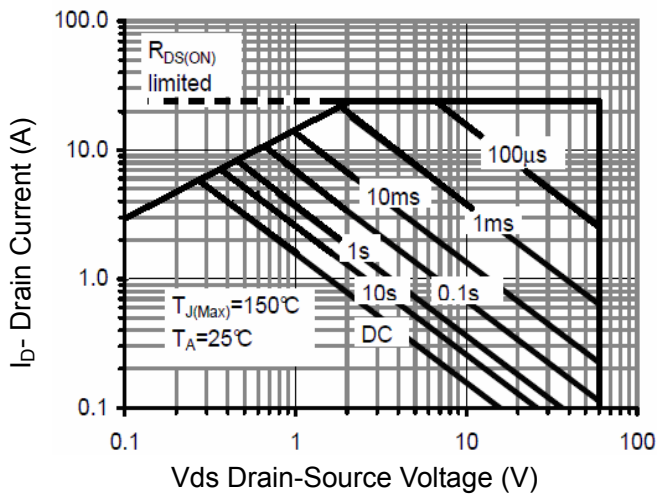

Figure 9  $BV_{DSS}$  vs Junction Temperature


Figure 8 Safe Operation Area

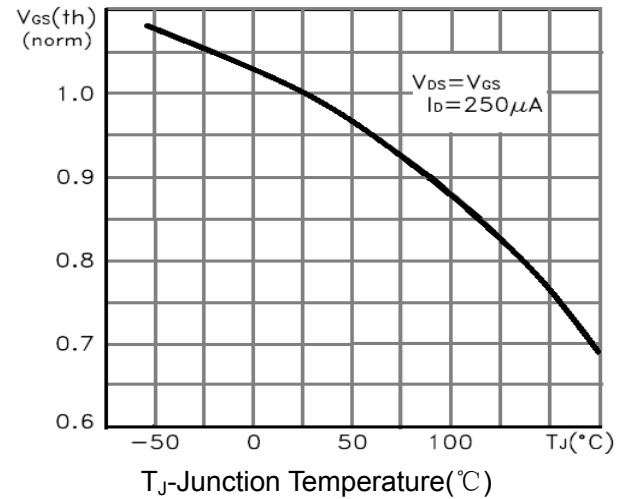
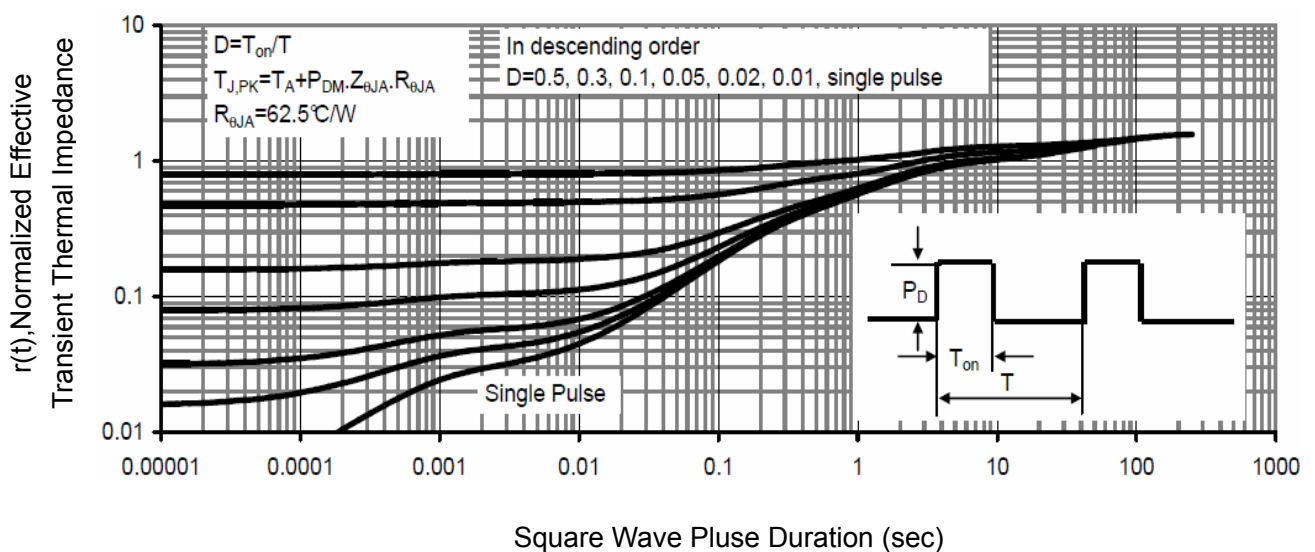
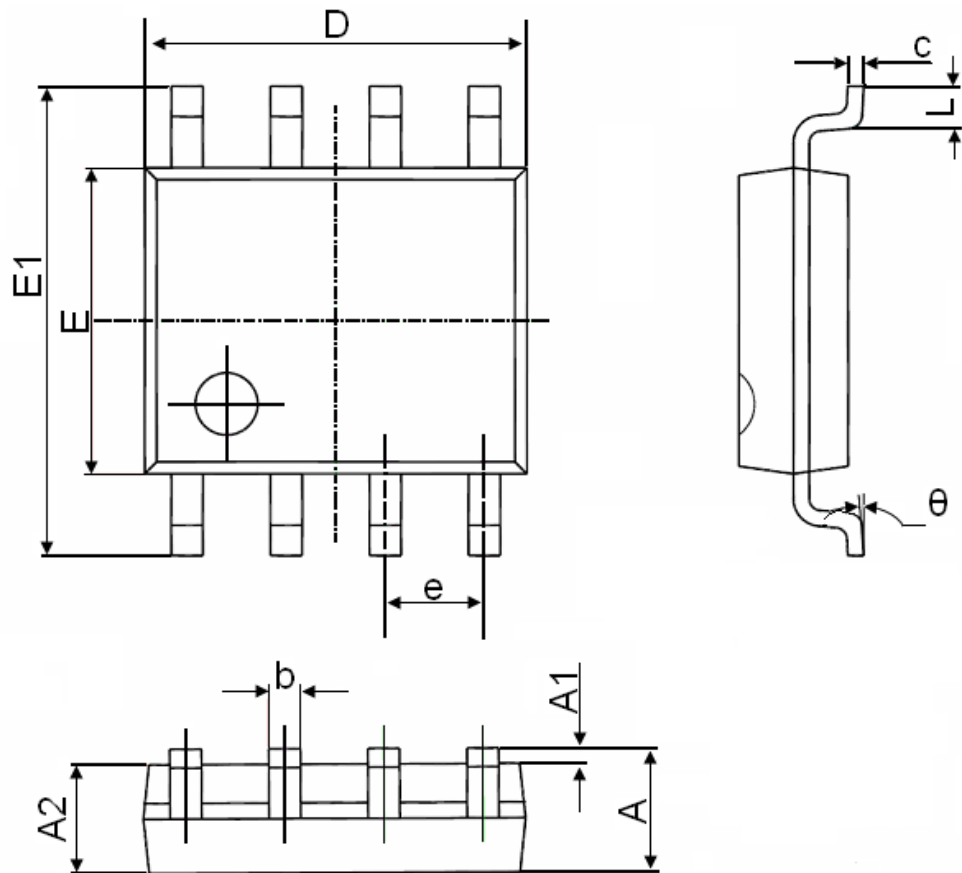

Figure 10  $V_{GS(th)}$  vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°