TGD N-Channel Enhancement Mode Power MOSFET
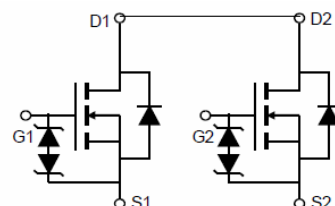
Description

The TGD8651Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.
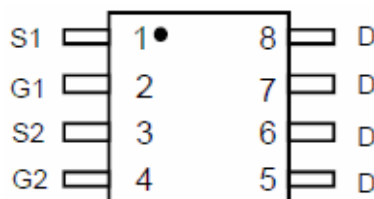
General Features

- V_{DS} =20V, I_D =10A

  $R_{DS(ON)}$ < 11mΩ @ V_{GS}=4.5V

  $R_{DS(ON)}$ < 11.5mΩ @ V_{GS}=4V

  $R_{DS(ON)}$ < 12.5mΩ @ V_{GS}=3.1V

  $R_{DS(ON)}$ < 15.5mΩ @ V_{GS}=2.5V

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
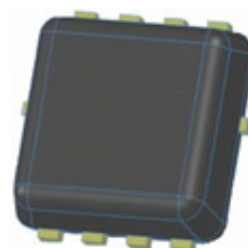- 2.5V Drive
- Common-drain type

Application

- Battery protection switch
- Mobile device battery charging and discharging

Schematic diagram

Pin Assignment

DFN 3x3 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD8651Q	TGD8651Q	DFN 3x3	-	-	-

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	10	A
Pulsed Drain Current	I_{DM}	32	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient [Note 2]	$R_{θJA}$	83	℃/W

Electrical Characteristics (TC=25℃ unless otherwise noted)

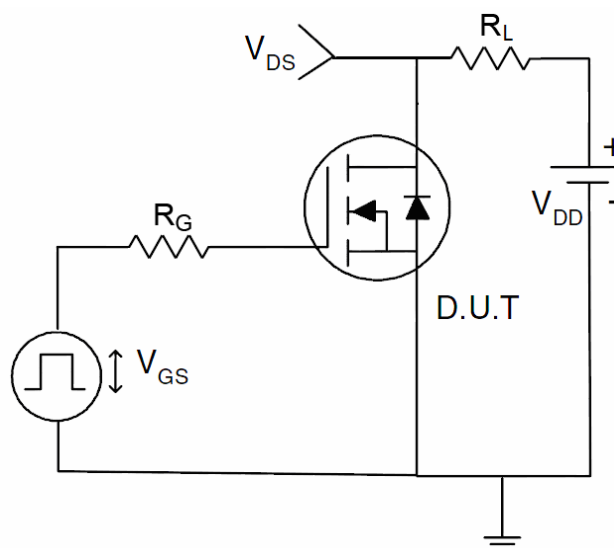| Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$ $I_D=250\mu A$	20		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	±10	μA
On Characteristics [Note 3]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=10A$	-	7.2	11	mΩ
		$V_{GS}=4 V, I_D=5A$	-	7.4	11.5	
		$V_{GS}=3.1V, I_D=5A$		7.8	12.5	
		$V_{GS}=2.5V, I_D=2.5A$		8.6	15.5	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=5A$	5	-	-	S
Dynamic Characteristics [Note4]						
Input Capacitance	C_{Iss}	$V_{DS}=10V, V_{GS}=0V,$ F=1.0MHz	-	1255	-	PF
Output Capacitance	C_{oss}		-	220	-	PF
Reverse Transfer Capacitance	C_{rss}		-	168	-	PF
Switching Characteristics [Note 4]						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=5A$ $V_{GS}=10V, R_{GEN}=50\Omega$	-	300	-	nS
Turn-on Rise Time	t_r		-	1000	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	4000	-	nS
Turn-Off Fall Time	t_f		-	2500	-	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=10A,$ $V_{GS}=10V$	-	29	-	nC
Gate-Source Charge	Q_{gs}		-	5.2	-	nC
Gate-Drain Charge	Q_{gd}		-	6.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage [Note 3]	V_{SD}	$V_{GS}=0V, I_S=10A$	-	0.85	1.2	V
Diode Forward Current [Note 2]	I_S		-	-	10	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

Test Circuit

1) Gate Charge Test Circuit

2) Switch Time Test Circuit

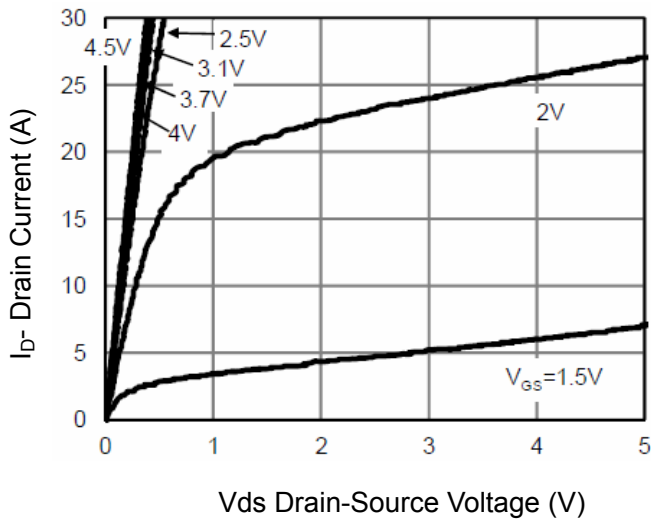## Typical Electrical and Thermal Characteristics (Curves)
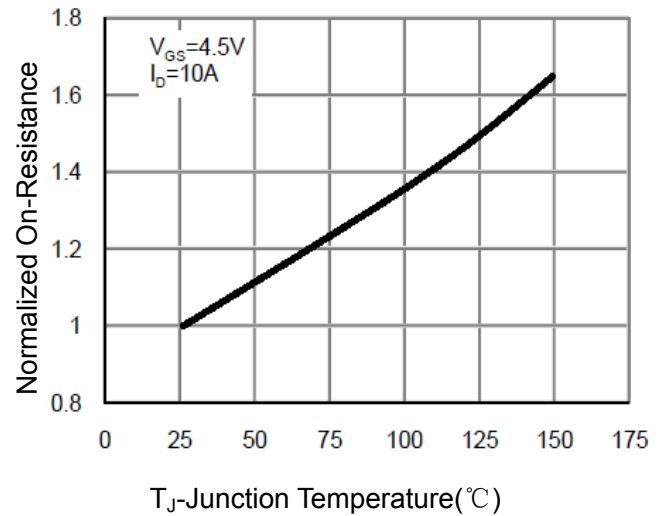

Figure 1 Output Characteristics
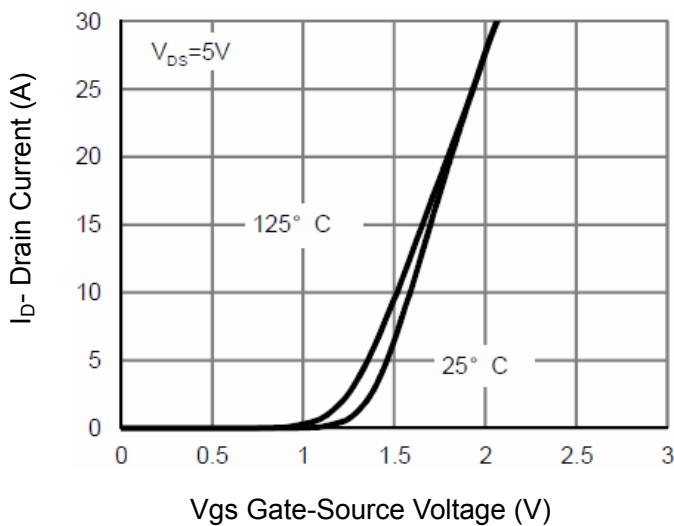

Figure 4 Rdson-Junction Temperature

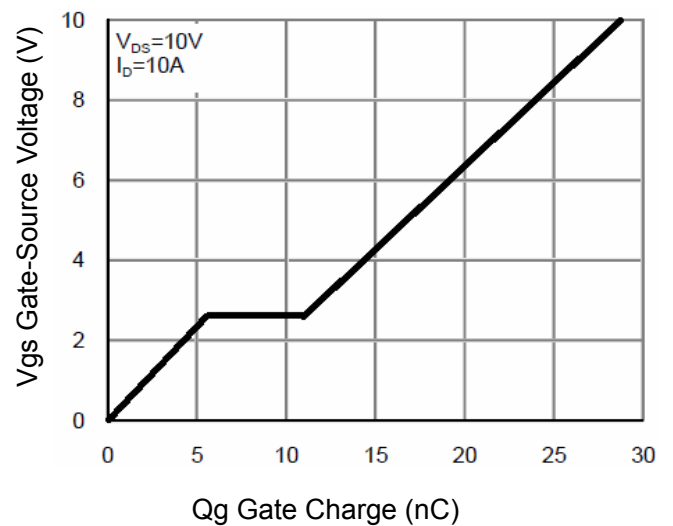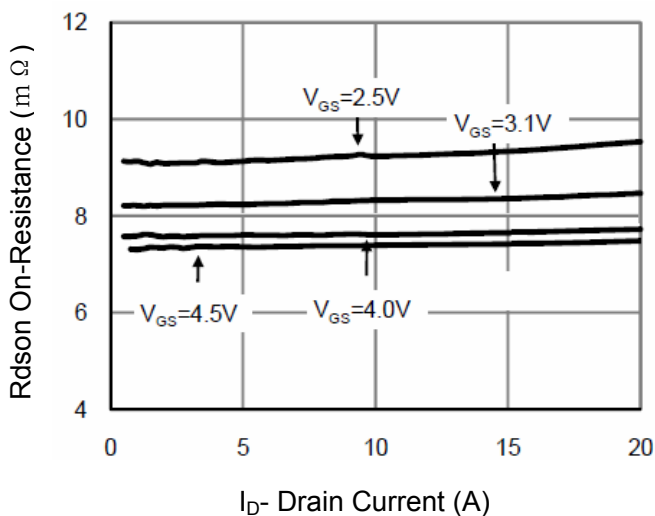

Figure 2 Transfer Characteristics

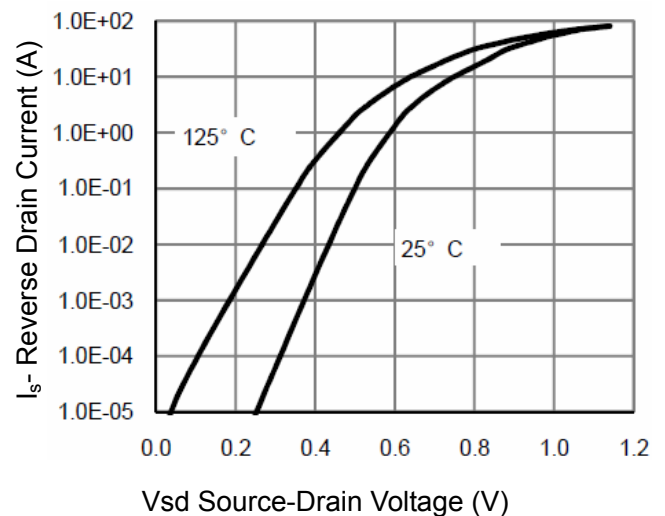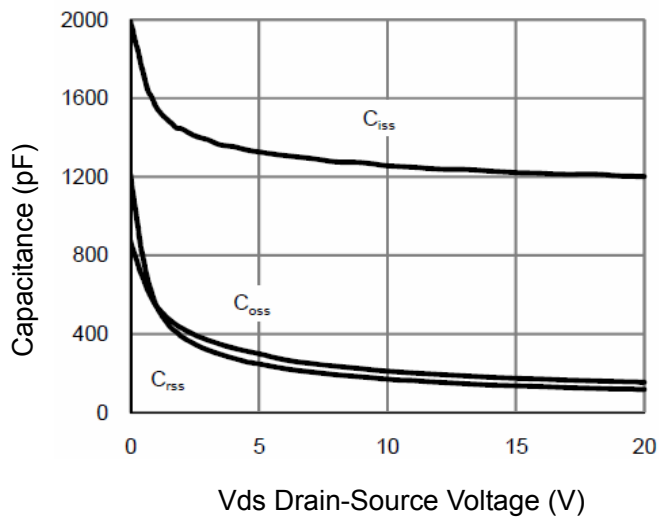**Figure 5 Gate Charge**

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward
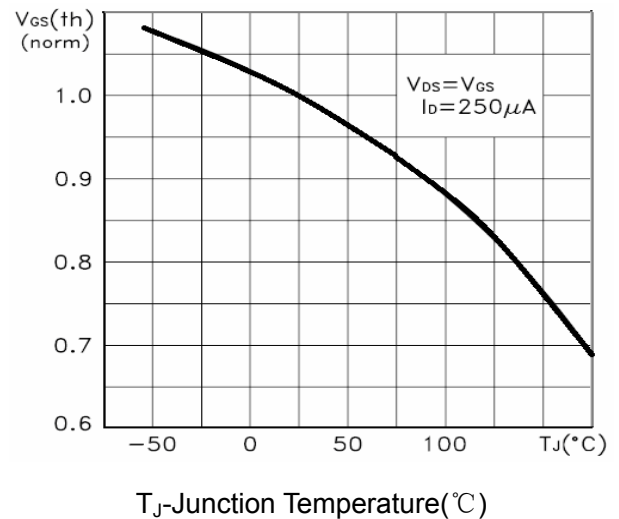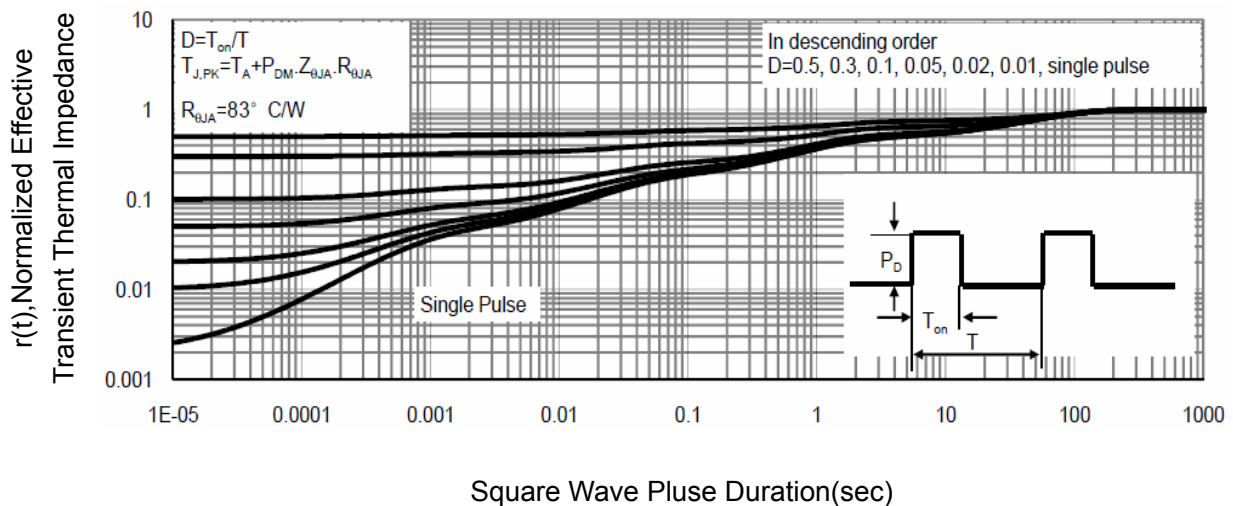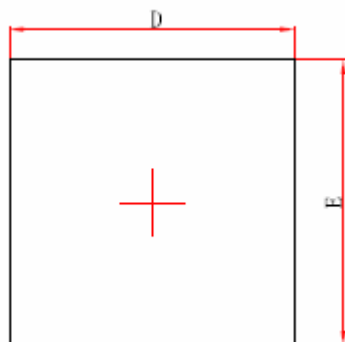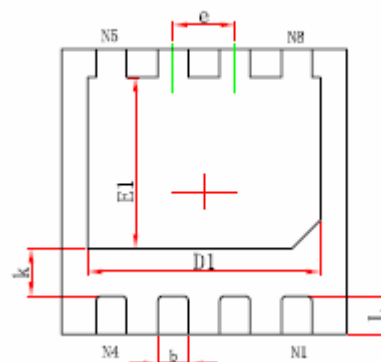
Figure 7 Capacitance vs Vds

Figure 9 BV$_{DSS}$ vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 V$_{GS(th)}$ vs Junction Temperature
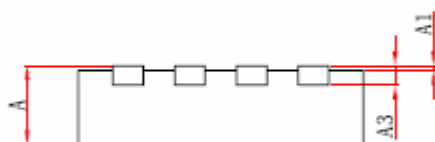

Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3X3 EP Package Information

Top View

Bottom View

Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.350	2.550	0.093	0.100
E1	1.700	1.900	0.067	0.075
k	0.450	0.550	0.018	0.022
b	0.270	0.370	0.011	0.015
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019