

## TGD N-Channel Enhancement Mode Power MOSFET

### Description

The TGD01H10 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

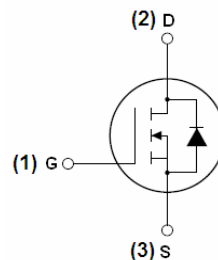
- $V_{DS} = 100V, I_D = 100A$   
 $R_{DS(ON)} < 13m\Omega @ V_{GS}=10V$  (Typ:9.9m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

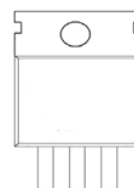
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**100% UIS TESTED!**

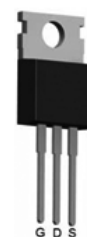
**100%  $\Delta V_{DS}$  TESTED!**



Schematic diagram



pin assignment



TO-220-3L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD01H10	TGD01H10	TO-220-3L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	100	A
$I_D (100^{\circ}C)$	Drain Current-Continuous( $T_C=100^{\circ}C$ )	80	A
$I_{DM}$	Pulsed Drain Current	380	A
$P_D$	Maximum Power Dissipation	200	W
	Derating factor	1.33	W/ $^{\circ}C$
$E_{AS}$	Single pulse avalanche energy <sup>(Note 5)</sup>	800	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^{\circ}C$

**Thermal Characteristic**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	0.75	$^{\circ}\text{C/W}$
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**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

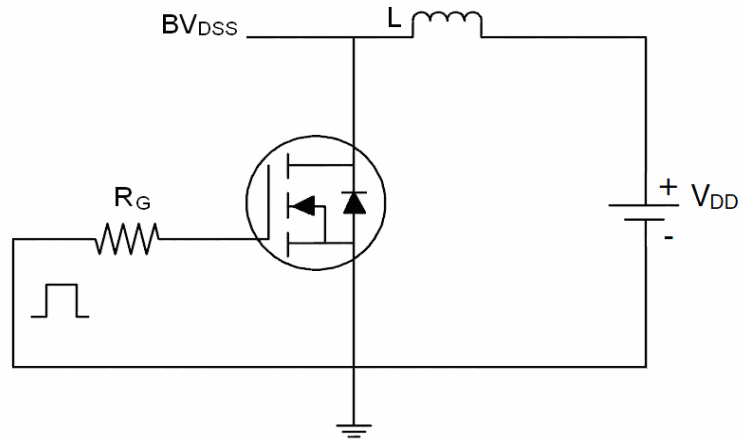
Symbol		Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage		V <sub>GS</sub> =0V I <sub>D</sub> =250μA	100	110	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	-	-	1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current		V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>							
V <sub>GS(th)</sub>	Gate Threshold Voltage		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance		V <sub>GS</sub> =10V, I <sub>D</sub> =40A	-	9.9	13	mΩ
g <sub>FS</sub>	Forward Transconductance		V <sub>DS</sub> =50V, I <sub>D</sub> =40A	100	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>							
C <sub>ISS</sub>	Input Capacitance		V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1.0MHz	-	4800	-	PF
C <sub>OSS</sub>	Output Capacitance			-	340	-	PF
C <sub>RSS</sub>	Reverse Transfer Capacitance			-	150	-	PF
Switching Characteristics <sup>(Note 4)</sup>							
t <sub>d(on)</sub>	Turn-on Delay Time		V <sub>DD</sub> =50V, I <sub>D</sub> =40A V <sub>GS</sub> =10V, R <sub>GEN</sub> =2.5Ω	-	15	-	nS
t <sub>r</sub>	Turn-on Rise Time			-	50	-	nS
t <sub>d(off)</sub>	Turn-Off Delay Time			-	40	-	nS
t <sub>f</sub>	Turn-Off Fall Time			-	55	-	nS
Q <sub>g</sub>	Total Gate Charge		V <sub>DS</sub> =80V, I <sub>D</sub> =40A, V <sub>GS</sub> =10V	-	85	-	nC
Q <sub>gs</sub>	Gate-Source Charge			-	18	-	nC
Q <sub>gd</sub>	Gate-Drain Charge			-	28	-	nC
Drain-Source Diode Characteristics							
V <sub>SD</sub>	Diode Forward Voltage <sup>(Note 3)</sup>		V <sub>GS</sub> =0V, I <sub>S</sub> =40A	-	-	1.2	V
I <sub>S</sub>	Diode Forward Current <sup>(Note 2)</sup>		-	-	-	57	A
t <sub>rr</sub>	Reverse Recovery Time		TJ = 25°C, IF = 40A	-	38	80	nS
Q <sub>rr</sub>	Reverse Recovery Charge		di/dt = 100A/μs(Note3)	-	53	100	nC
t <sub>on</sub>	Forward Turn-On Time		Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

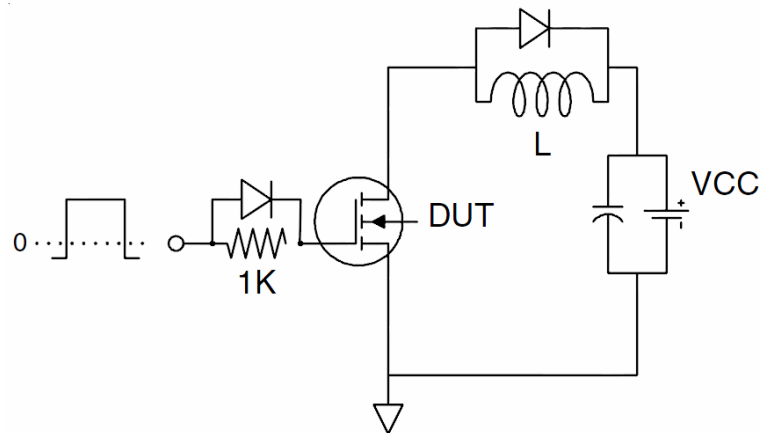
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

## Test Circuit

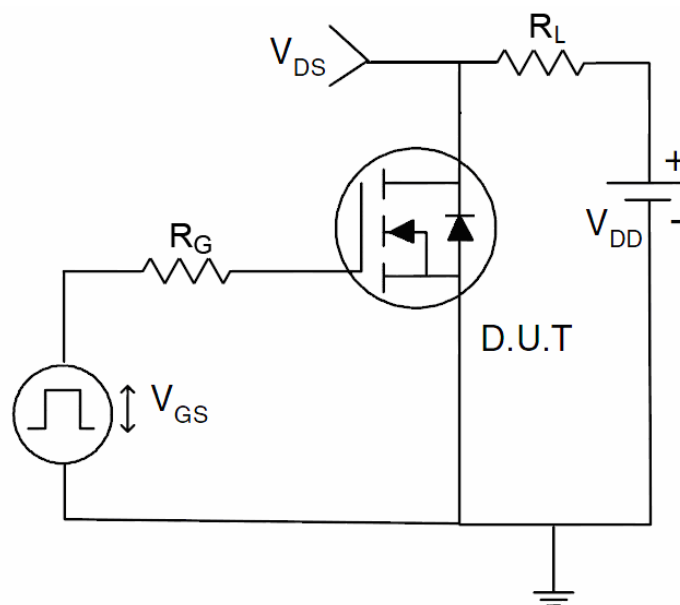
### 1) $E_{AS}$ test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit



# Typical Electrical and Thermal Characteristics (Curves)

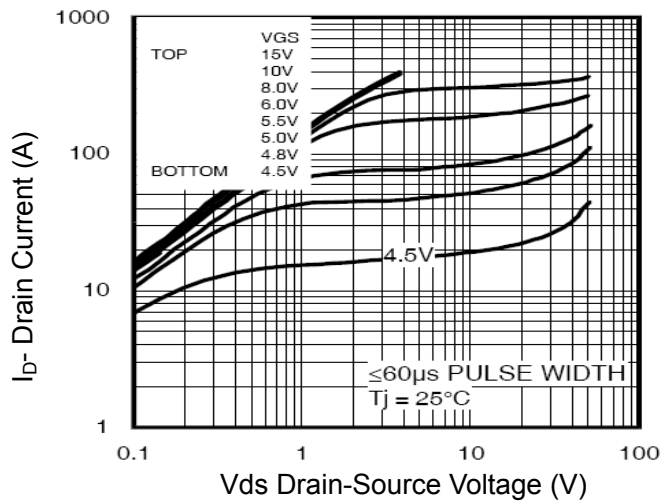


Figure 1 Output Characteristics

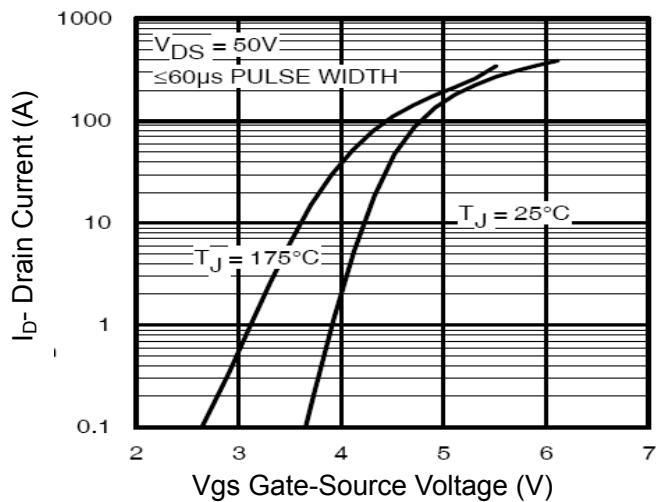


Figure 2 Transfer Characteristics

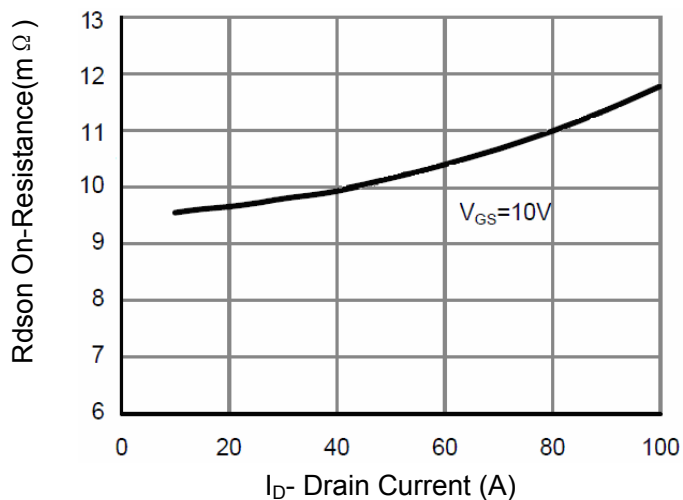


Figure 3 Rdson- Drain Current

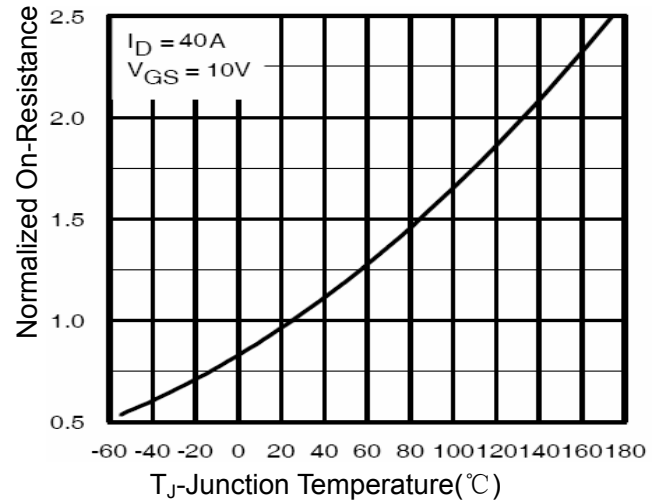


Figure 4 Rdson-Junction Temperature

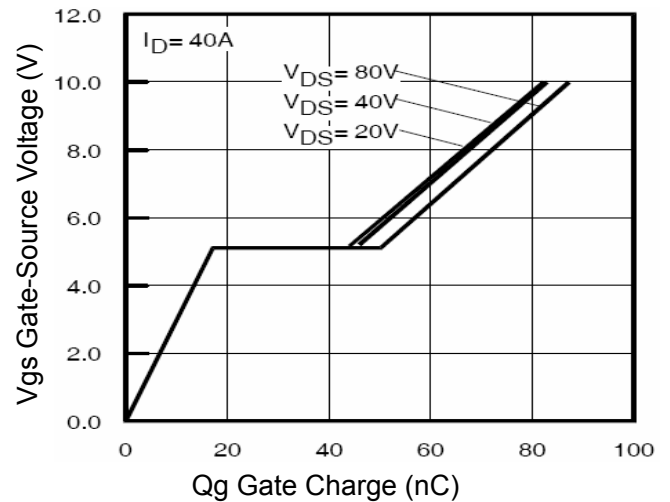


Figure 5 Gate Charge

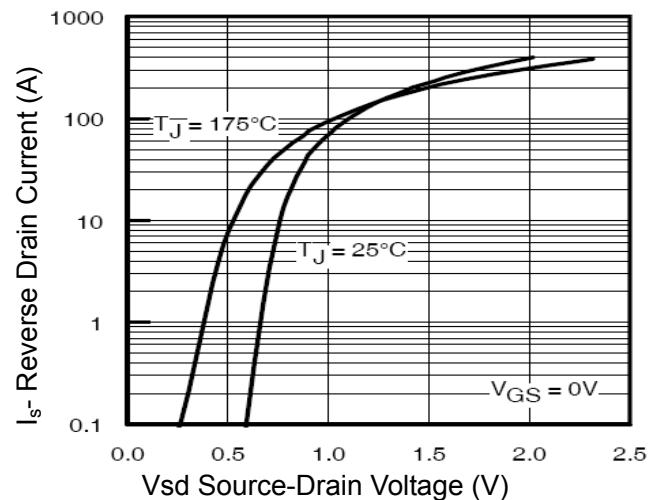


Figure 6 Source- Drain Diode Forward

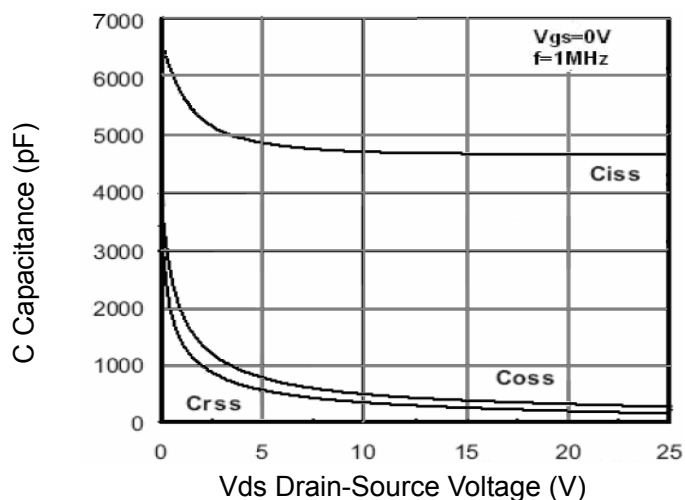


Figure 7 Capacitance vs Vds

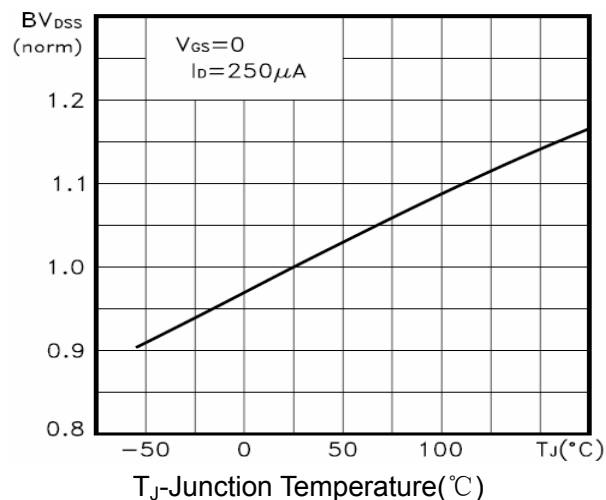
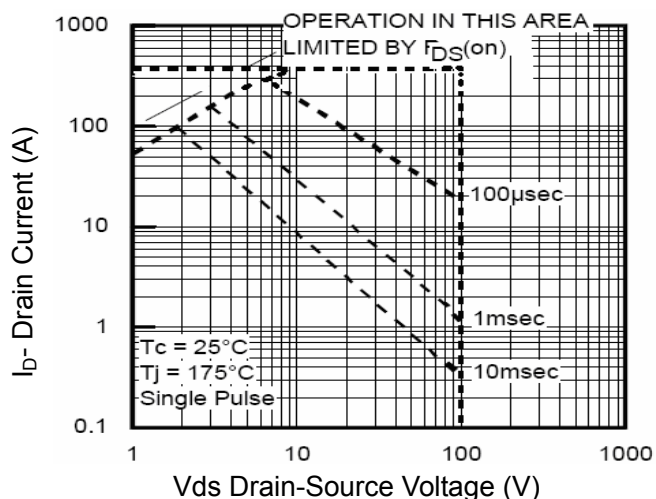

Figure 9  $BV_{DSS}$  vs Junction Temperature


Figure 8 Safe Operation Area

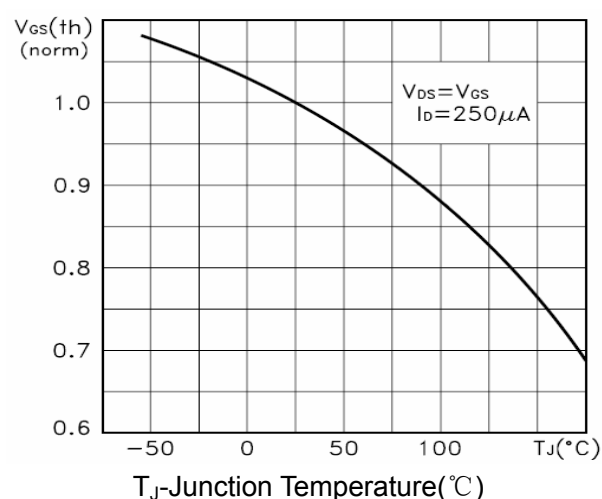
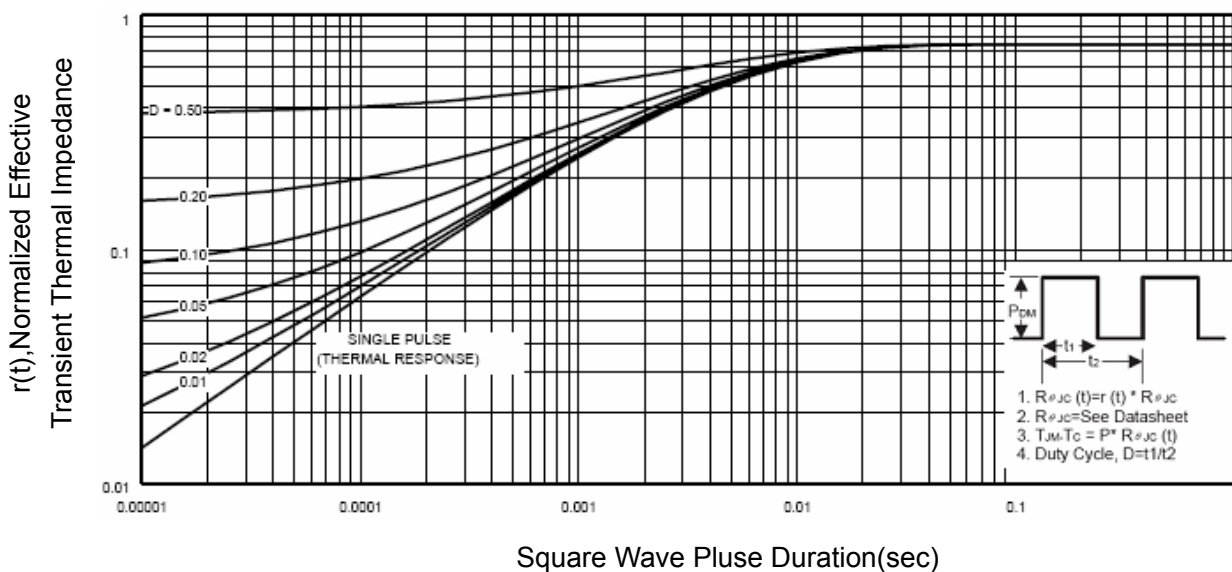
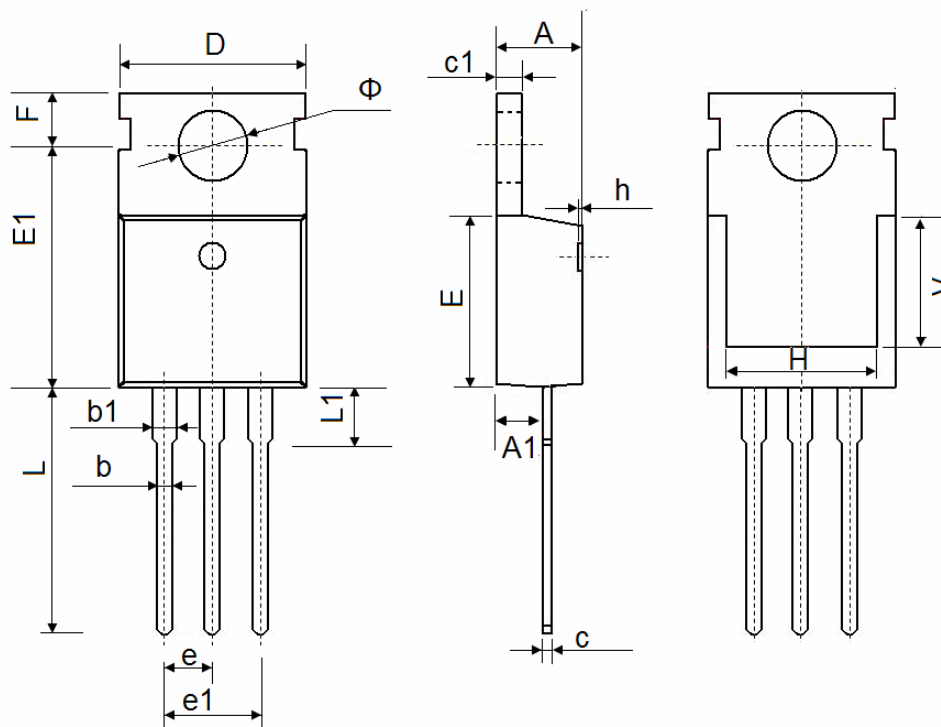

Figure 10  $V_{GS(th)}$  vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance

## TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150