

**TGD N-Channel Super Trench Power MOSFET****Description**

The TGDP85T12 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

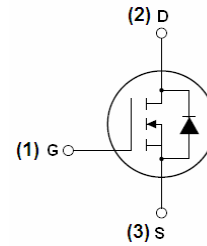
- $V_{DS} = 85V, I_D = 120A$
 $R_{DS(ON)} < 5.3m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

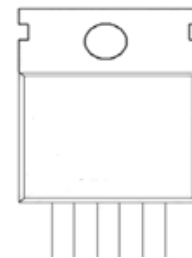
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!

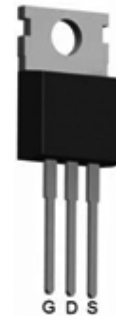
100% ΔV_{ds} TESTED!



Schematic diagram



pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGDP85T12	TGDP85T12	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	85	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	120	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	88	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	160	W
Derating factor		1.1	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	784	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.94	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

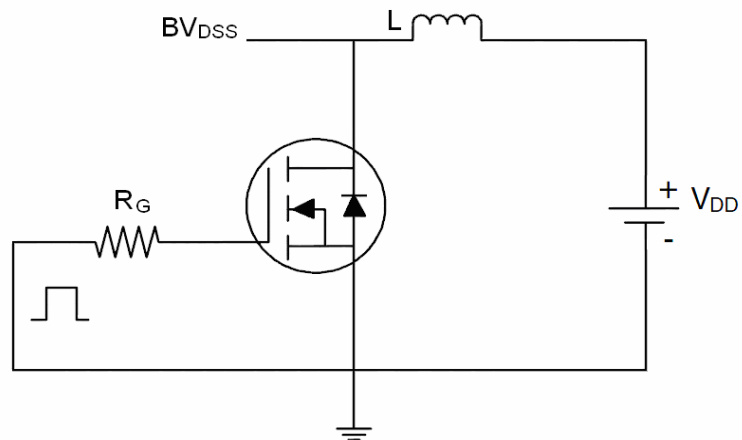
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	85		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =85V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5	-	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =60A	-	4.5	5.3	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =60A	40	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =40V, V _{GS} =0V, F=1.0MHz	-	5500	-	PF
Output Capacitance	C _{oss}		-	830	-	PF
Reverse Transfer Capacitance	C _{rss}		-	57	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =40V, I _D =60A V _{GS} =10V, R _G =4.7Ω	-	13.5	-	nS
Turn-on Rise Time	t _r		-	12.5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	38	-	nS
Turn-Off Fall Time	t _f		-	13.5	-	nS
Total Gate Charge	Q _g	V _{DS} =40V, I _D =60A, V _{GS} =10V	-	55		nC
Gate-Source Charge	Q _{gs}		-	21		nC
Gate-Drain Charge	Q _{gd}		-	9		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =120A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	120	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs (Note3)	-	74		nS
Reverse Recovery Charge	Q _{rr}		-	176		nC

Notes:

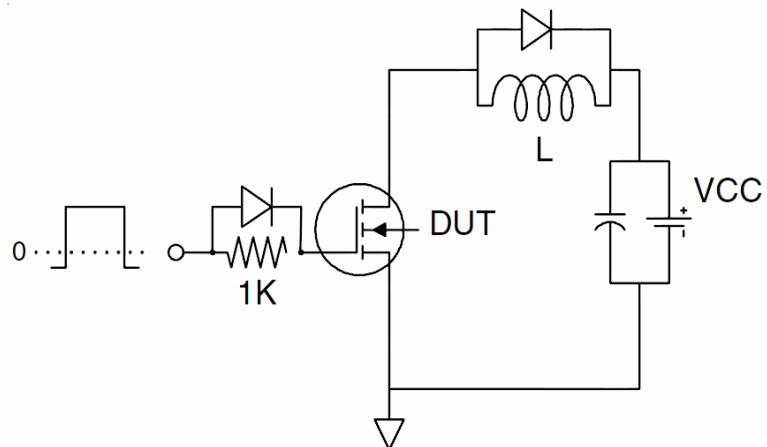
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=42.5V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

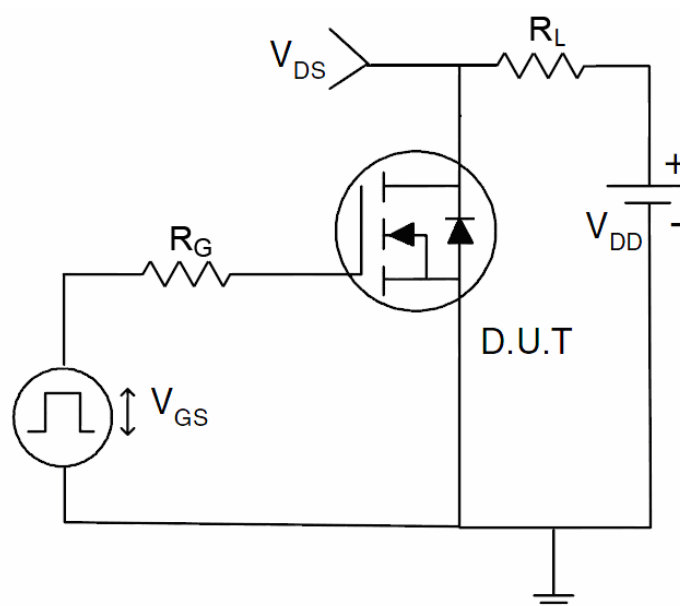
1) E_{AS} test Circuit



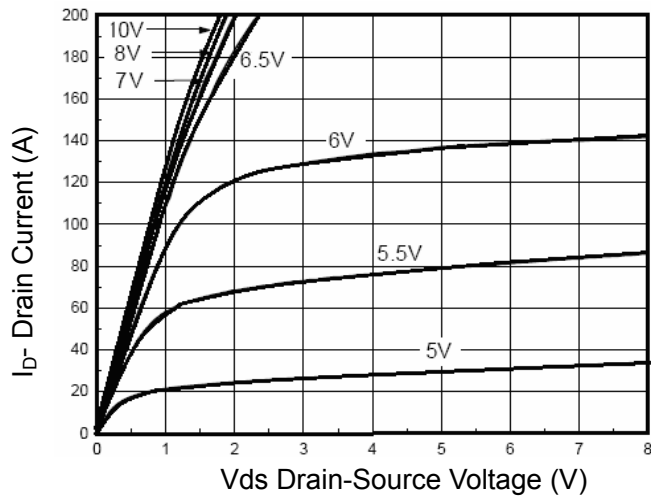
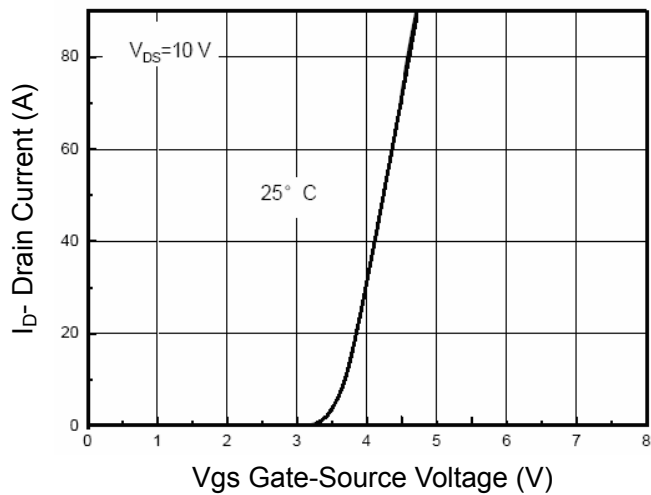
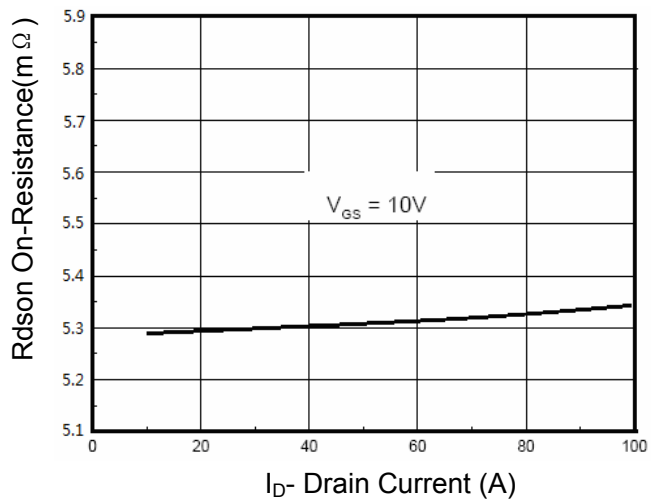
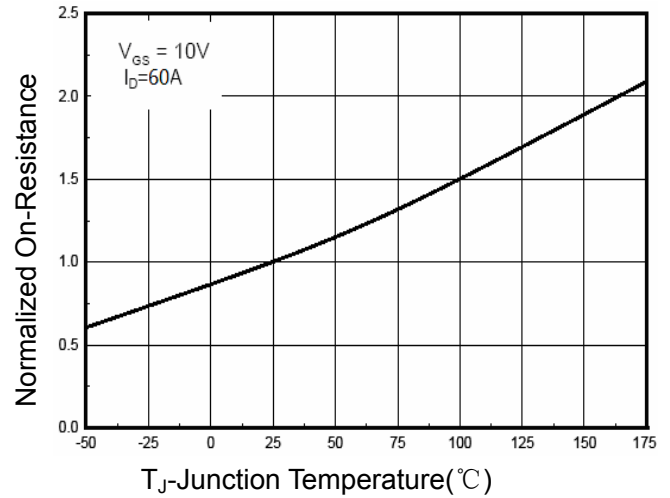
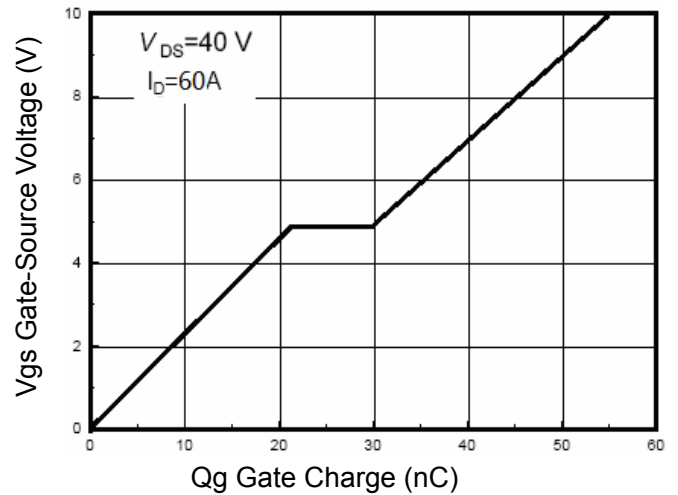
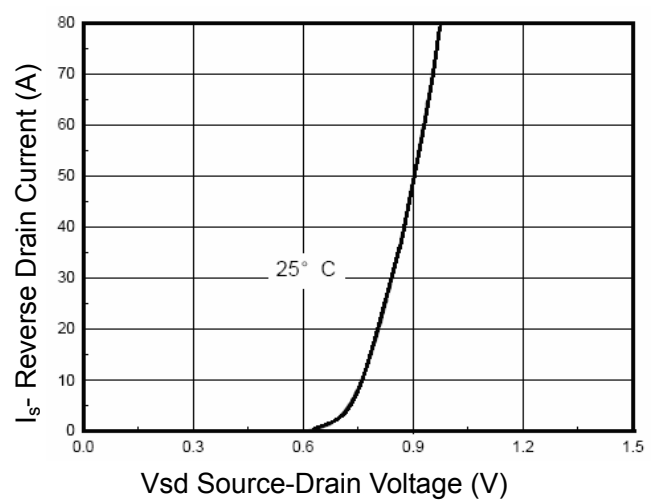
2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics


Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 Rdson- Drain Current

Figure 4 Rdson-Junction Temperature

Figure 5 Gate Charge

Figure 6 Source- Drain Diode Forward

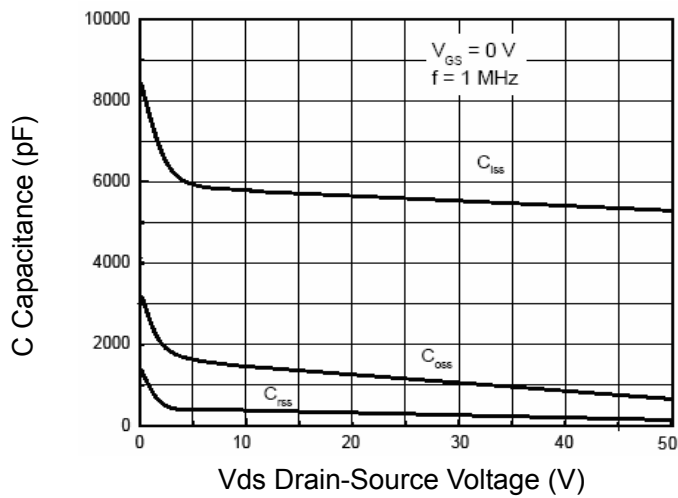


Figure 7 Capacitance vs Vds

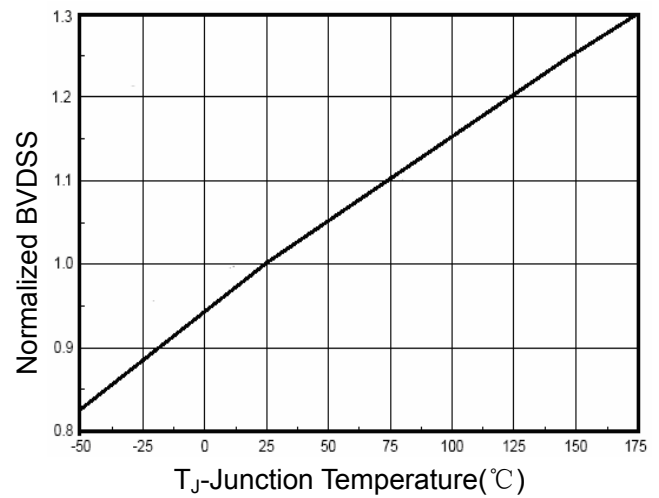
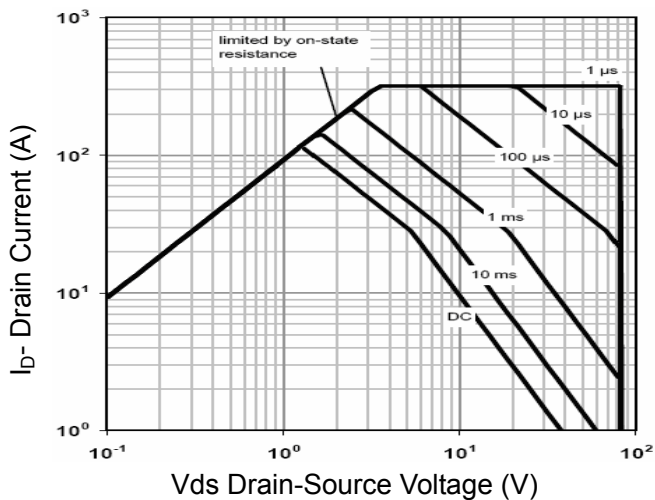

Figure 9 BV_{DSS} vs Junction Temperature


Figure 8 Safe Operation Area

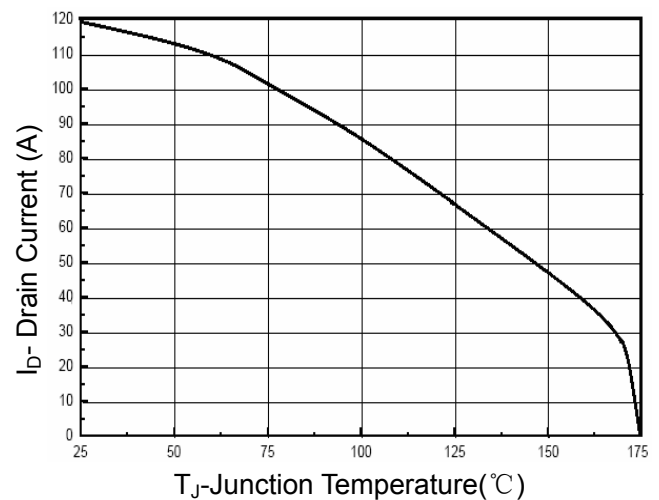


Figure 10 Current De-rating

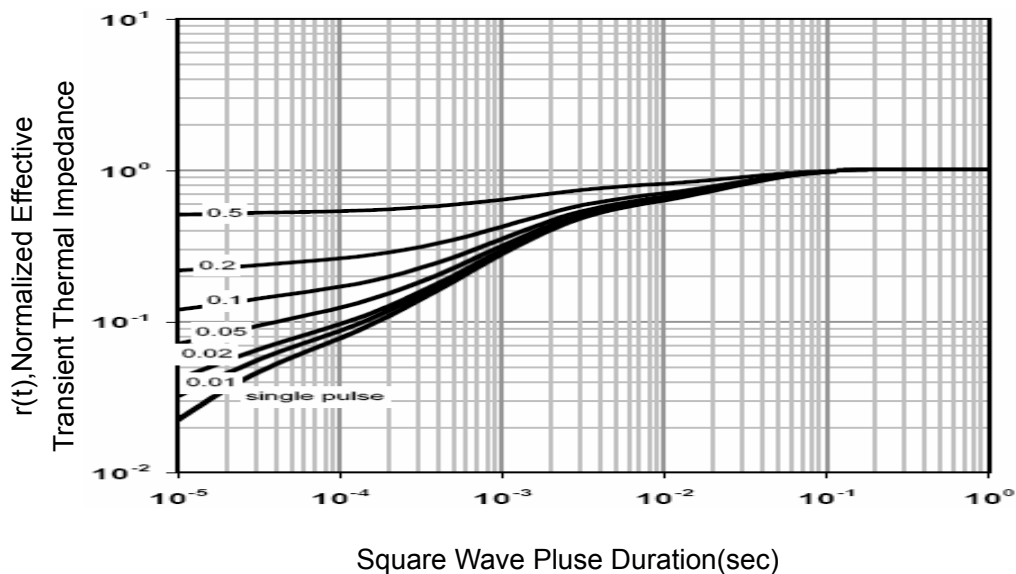
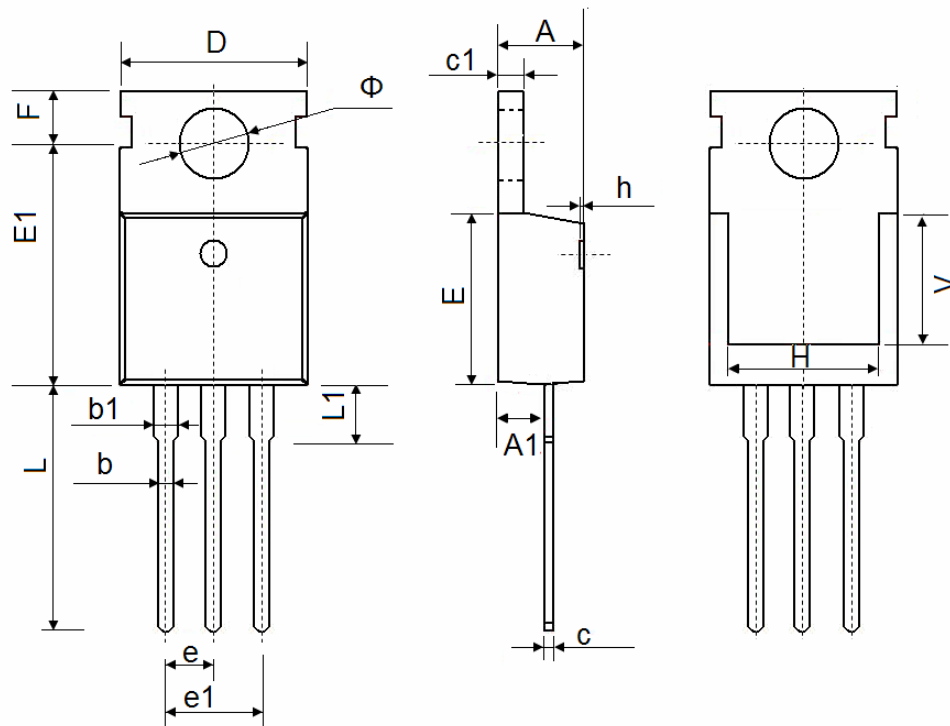


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150