

## TGD N-Channel Enhancement Mode Power MOSFET

### Description

The TGD1450 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

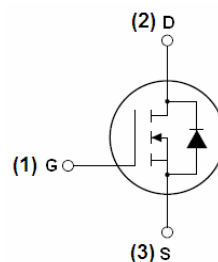
- $V_{DS}=140V, I_D=50A$   
 $R_{DS(ON)} < 28m\Omega @ V_{GS}=10V$  (Typ:24.5m $\Omega$ )
- High density cell design for ultra low  $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

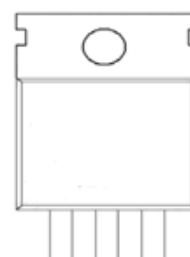
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**100% UIS TESTED!**

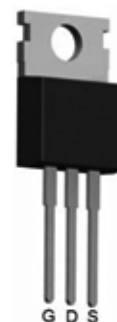
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



pin assignment



TO-220-3L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
1450	1450	TO-220-3L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	140	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	50	A
Drain Current-Continuous( $T_C=100^{\circ}C$ )	$I_D(100^{\circ}C)$	35	A
Pulsed Drain Current	$I_{DM}$	164	A
Maximum Power Dissipation	$P_D$	150	W
Derating factor		1	W/ $^{\circ}C$
Single pulse avalanche energy (Note 5)	$E_{AS}$	310	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^{\circ}C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.0	$^{\circ}\text{C/W}$
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**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

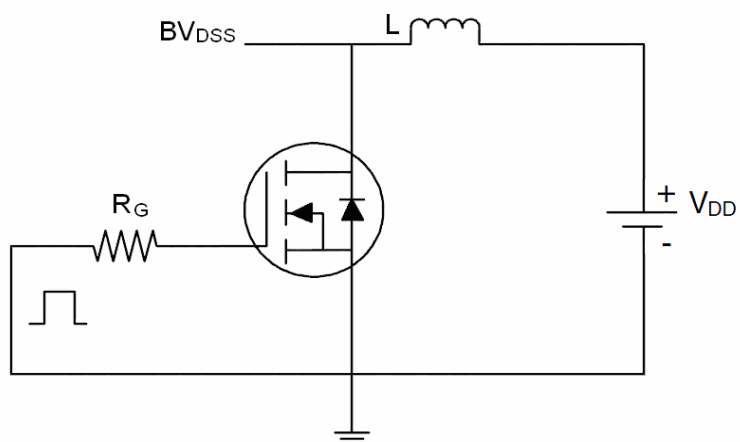
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	140	150	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =140V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	24.5	28	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	30	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	3520	-	PF
Output Capacitance	C <sub>OSS</sub>		-	203	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	96	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =2A, R <sub>L</sub> =15Ω V <sub>GS</sub> =10V, R <sub>G</sub> =2.5Ω	-	17.8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	11.8	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	56	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	14.6	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V		105	-	nC
Gate-Source Charge	Q <sub>gs</sub>			21	-	nC
Gate-Drain Charge	Q <sub>gd</sub>			31.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	0.80	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	50	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs <sup>(Note3)</sup>	-	70	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	130	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

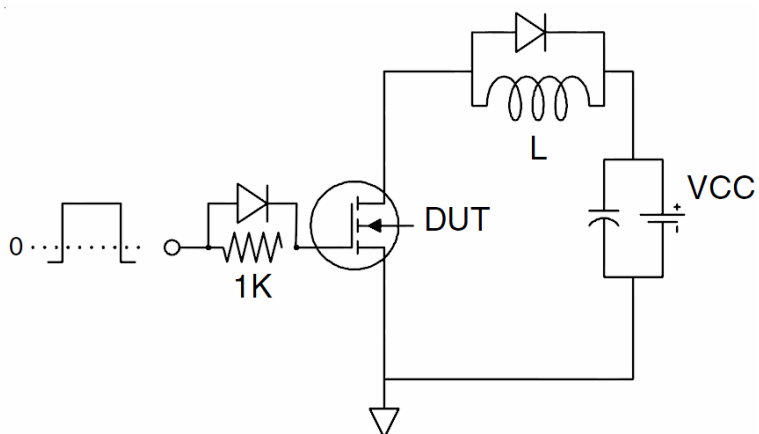
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}$ ,  $V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25\Omega$

## Test Circuit

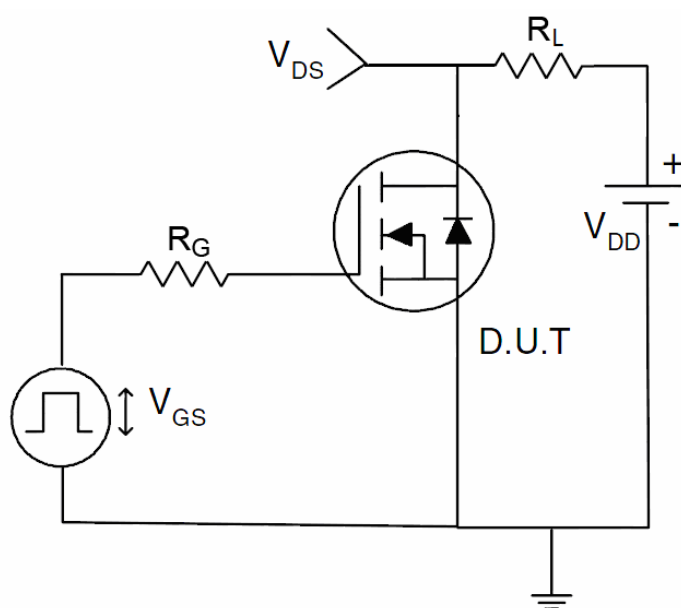
### 1) $E_{AS}$ test Circuit



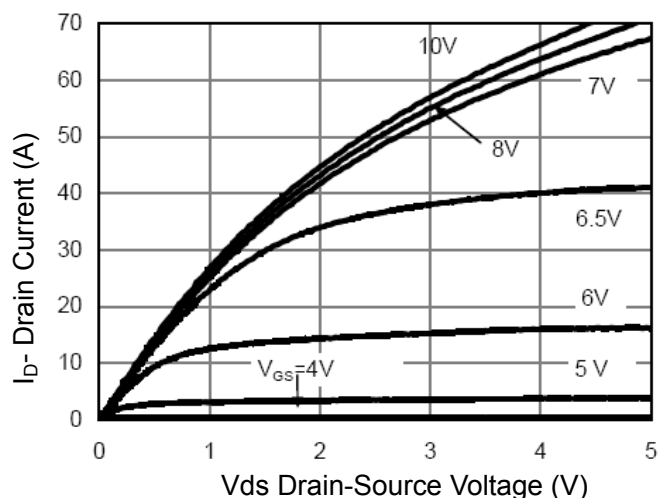
### 2) Gate charge test Circuit



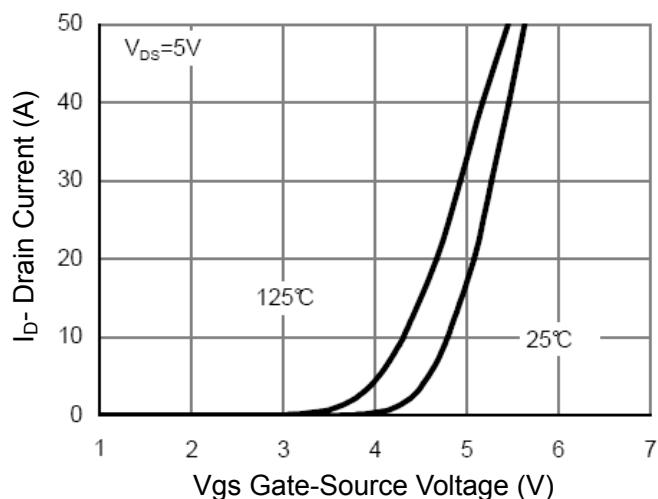
### 3) Switch Time Test Circuit



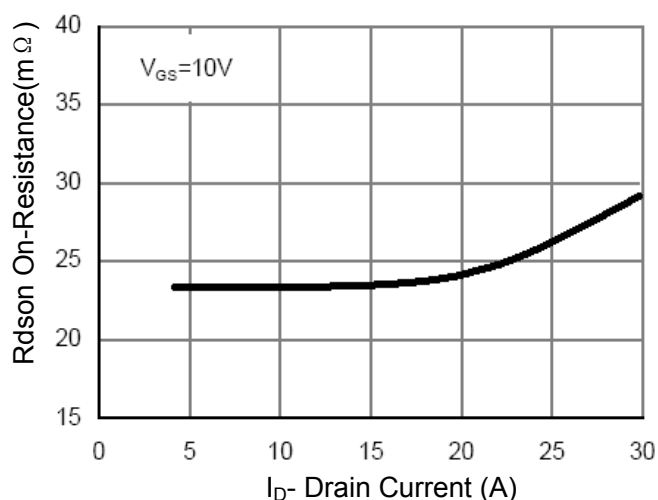
## Typical Electrical and Thermal Characteristics (Curves)



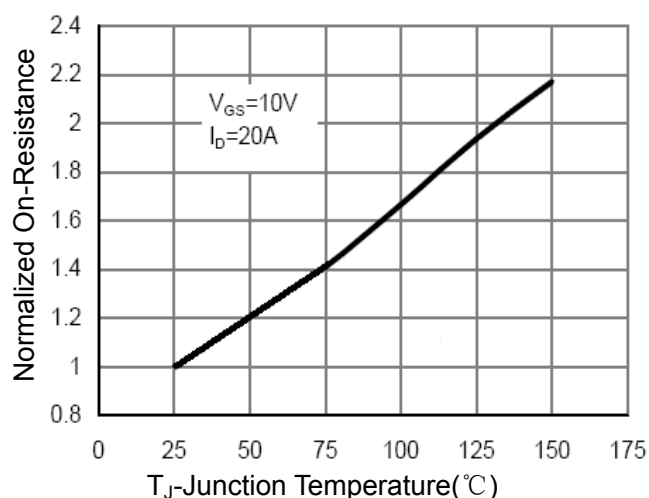
**Figure 1 Output Characteristics**



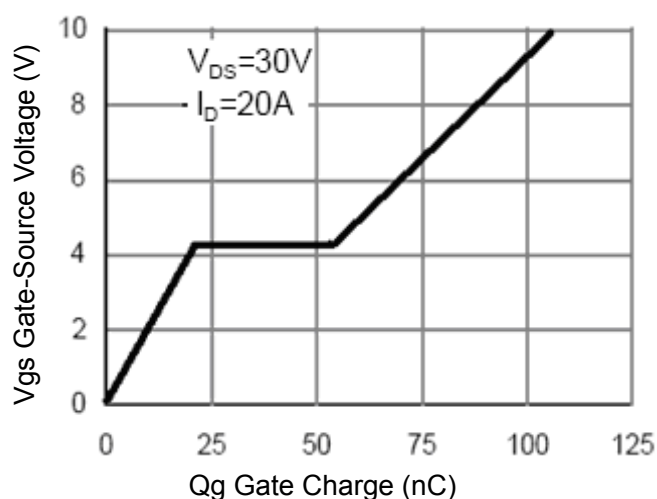
**Figure 2 Transfer Characteristics**



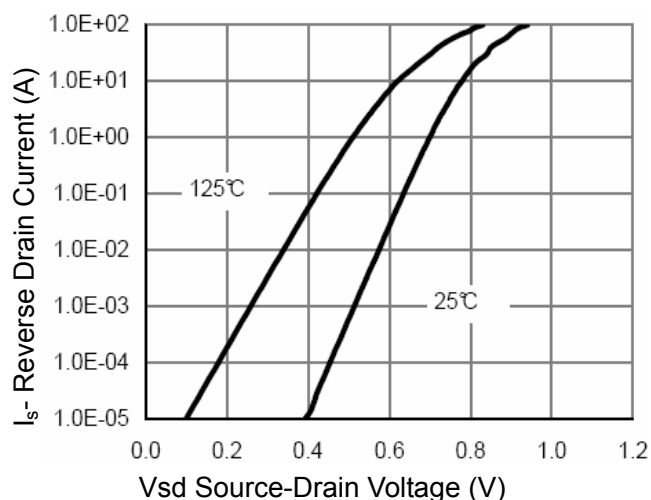
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

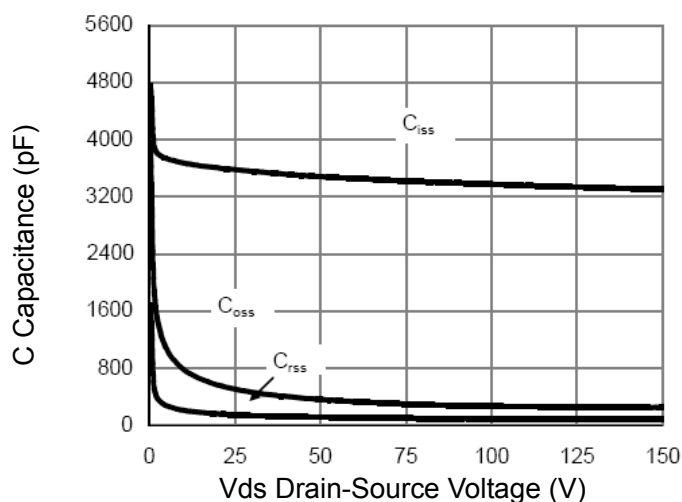


Figure 7 Capacitance vs Vds

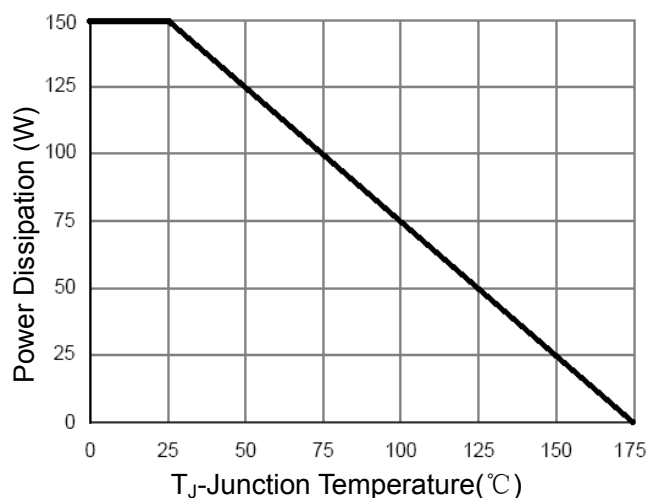


Figure 9 Power De-rating

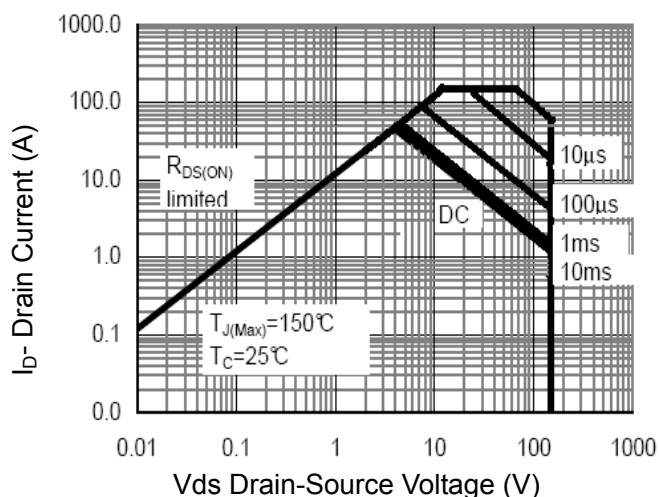


Figure 8 Safe Operation Area

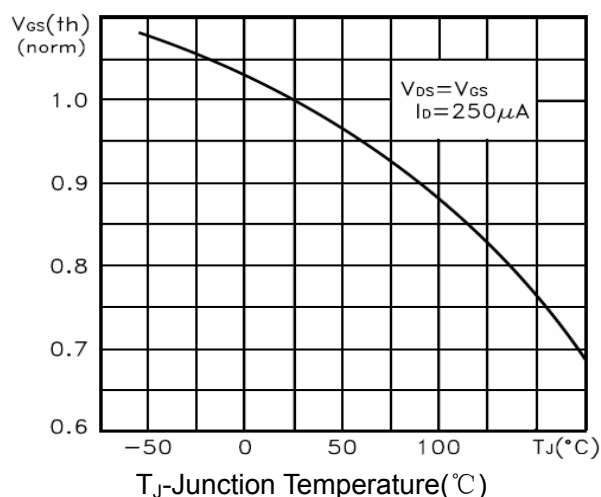
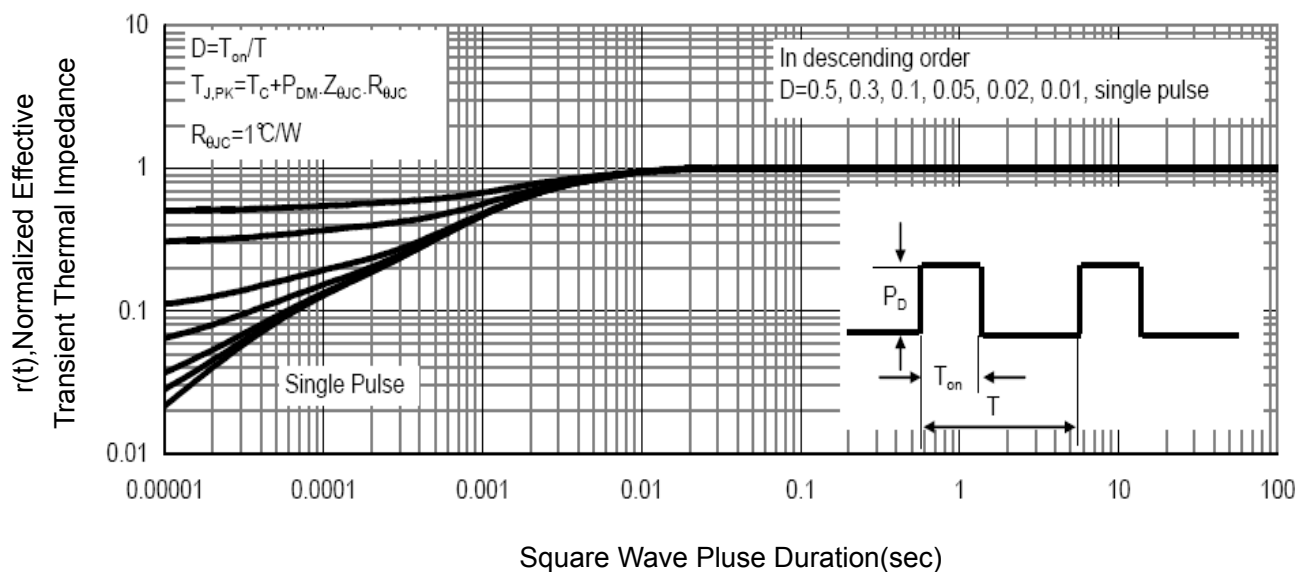
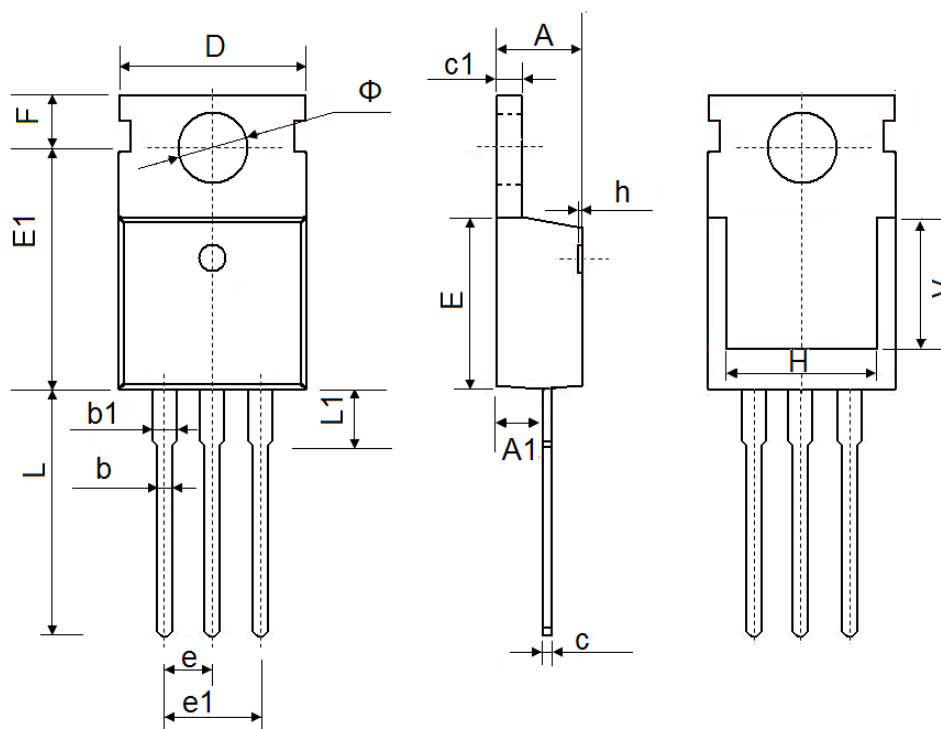

Figure 10  $V_{GS(th)}$  vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance

## TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150