

TGD N-Channel Enhancement Mode Power MOSFET

Description

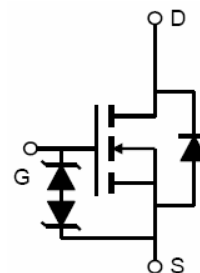
The TGD2014ES uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

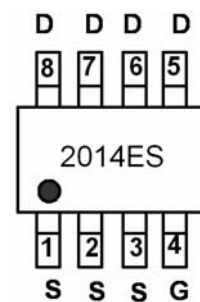
- $V_{DS} = 20V, I_D = 14A$
 $R_{DS(ON)} < 7 m\Omega @ V_{GS} = 4.5V$
 $R_{DS(ON)} < 9 m\Omega @ V_{GS} = 2.5V$
ESD Rating: 2000V HBM
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

Application

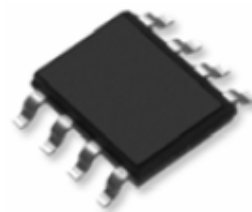
- PWM application
- Load switch



Schematic diagram



pin Assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
2014ES	TGD2014ES	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	44	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	42	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

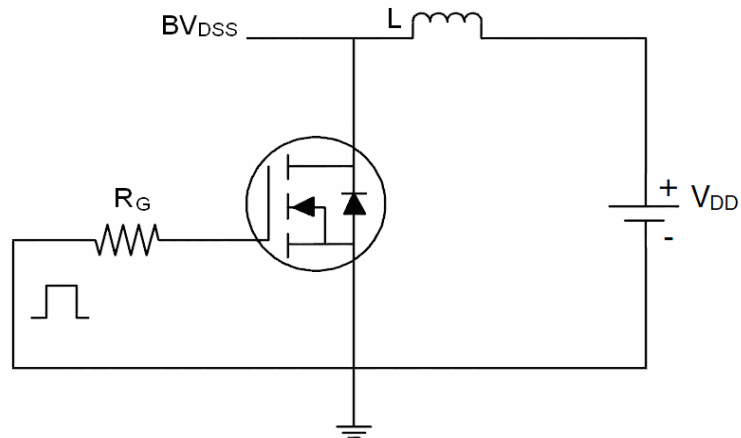
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	22	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	± 10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6	0.8	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=10A$	-	5	7	m Ω
		$V_{GS}=2.5V, I_D=5.5A$	-	7	9	
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=10A$	30	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	1710	-	PF
Output Capacitance	C_{oss}		-	232	-	PF
Reverse Transfer Capacitance	C_{rss}		-	200	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	2.5	-	nS
Turn-on Rise Time	t_r		-	7.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	49	-	nS
Turn-Off Fall Time	t_f		-	10.8	-	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=10A,$ $V_{GS}=4.5V$	-	17.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain Charge	Q_{gd}		-	4.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	14	A

Notes:

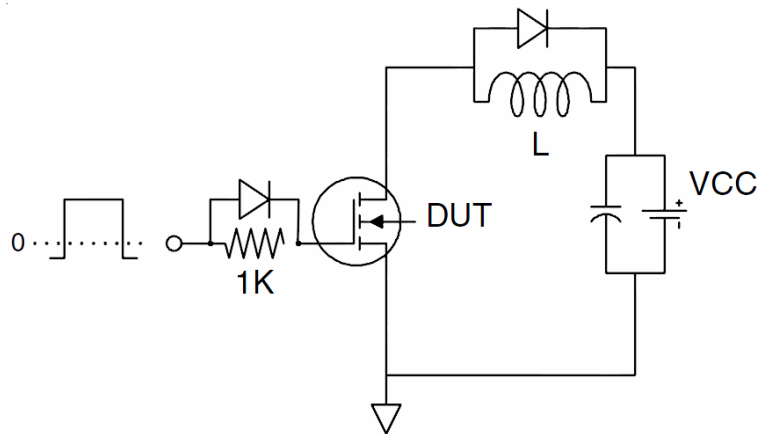
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

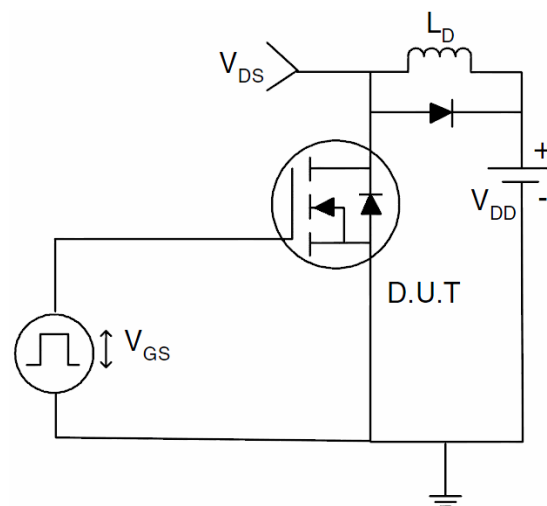
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

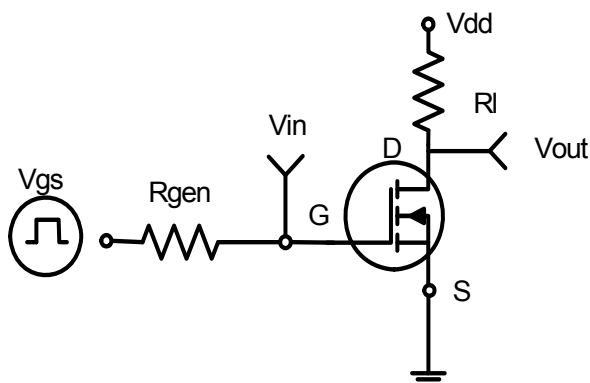


Figure 1: Switching Test Circuit

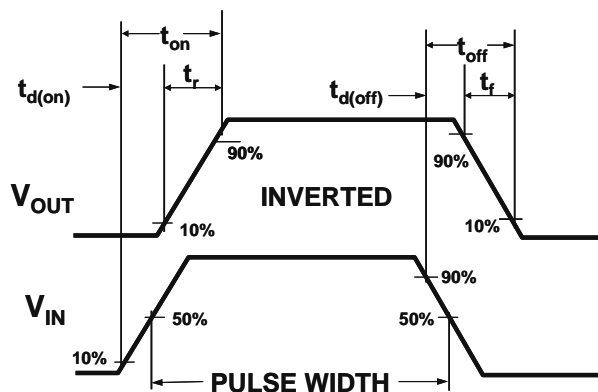


Figure 2: Switching Waveforms

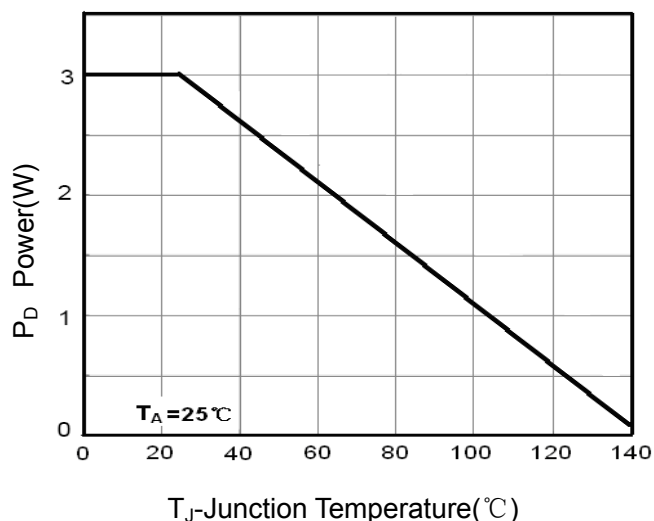


Figure 3 Power Dissipation

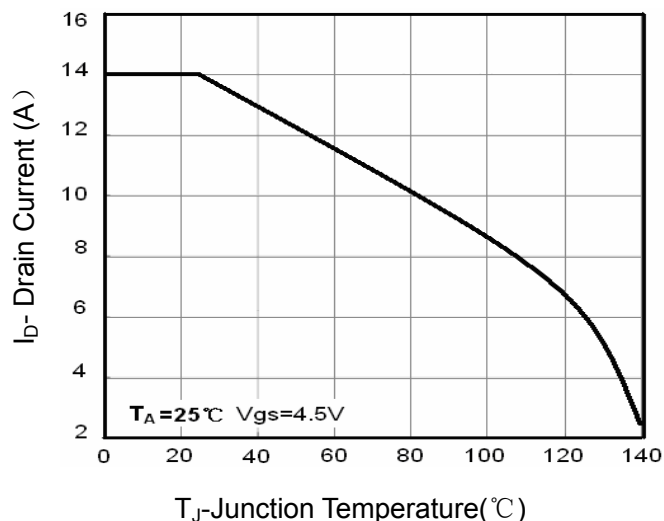


Figure 4 Drain Current

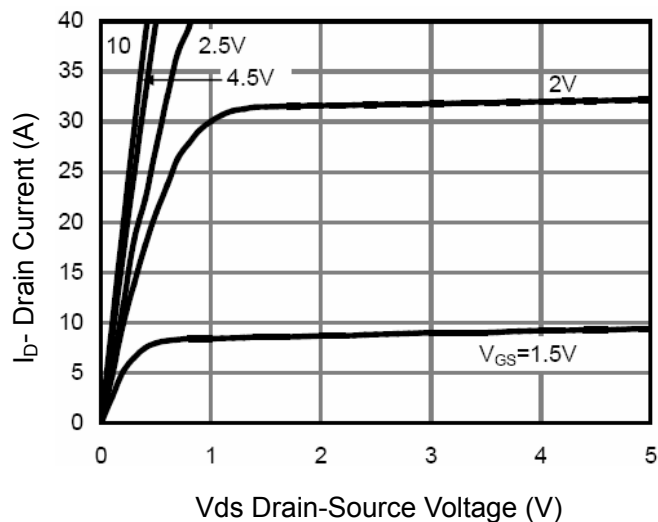


Figure 5 Output Characteristics

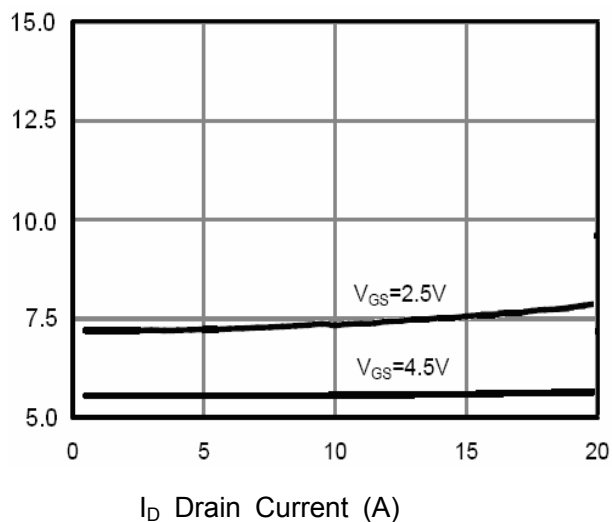
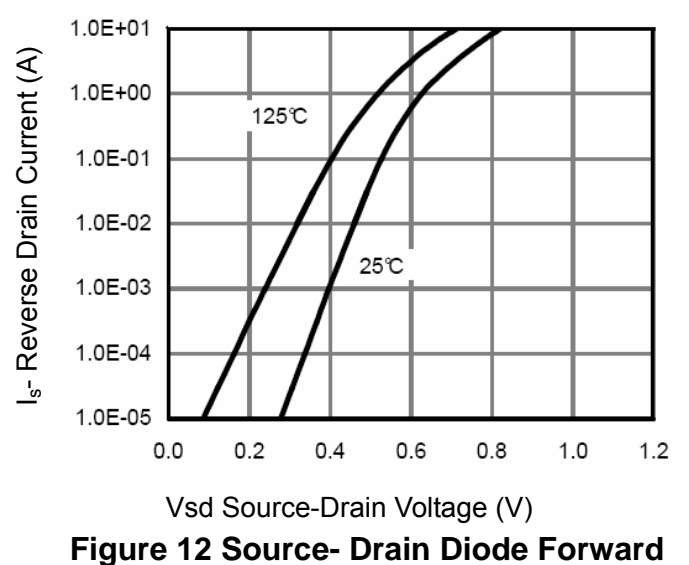
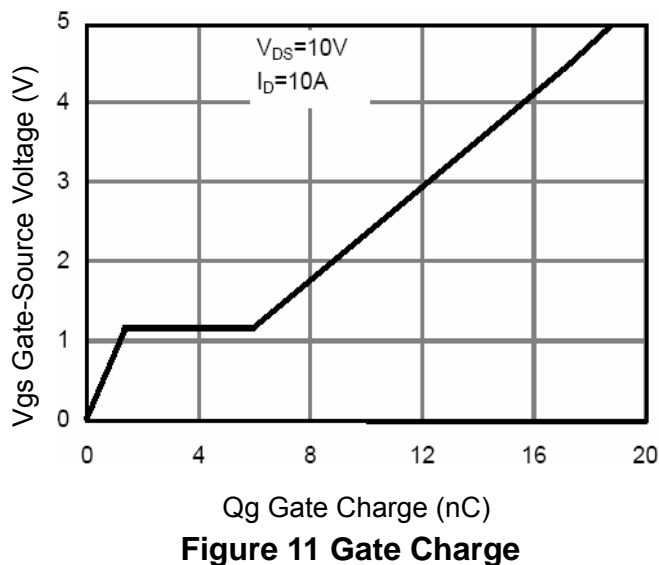
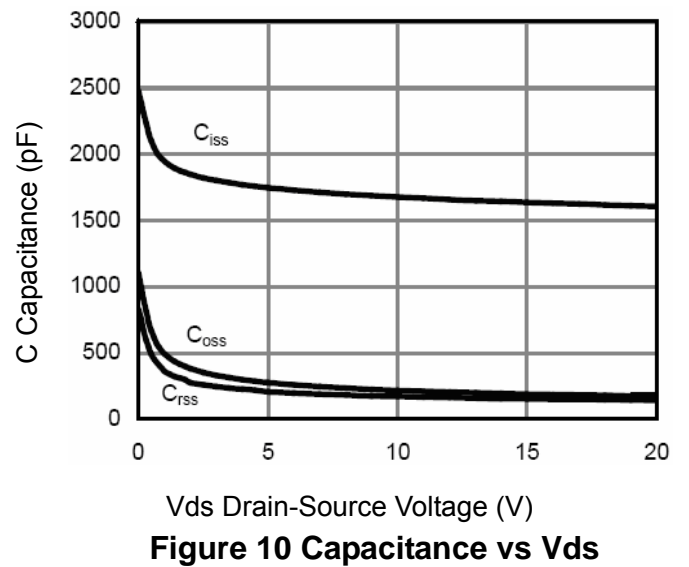
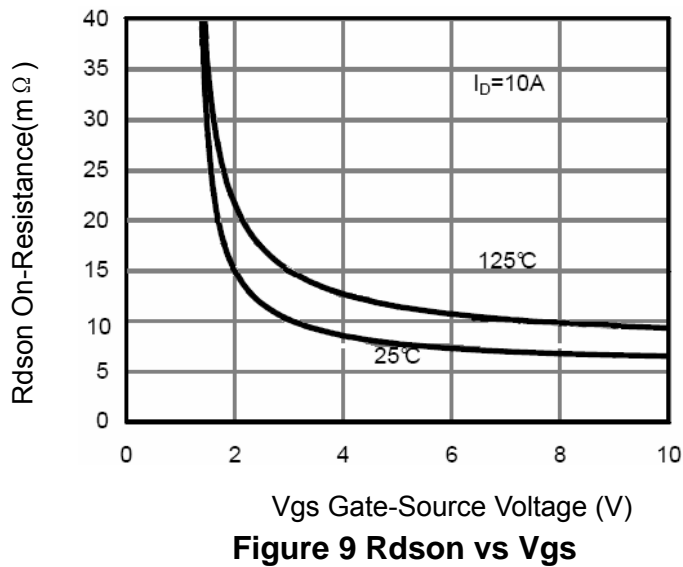
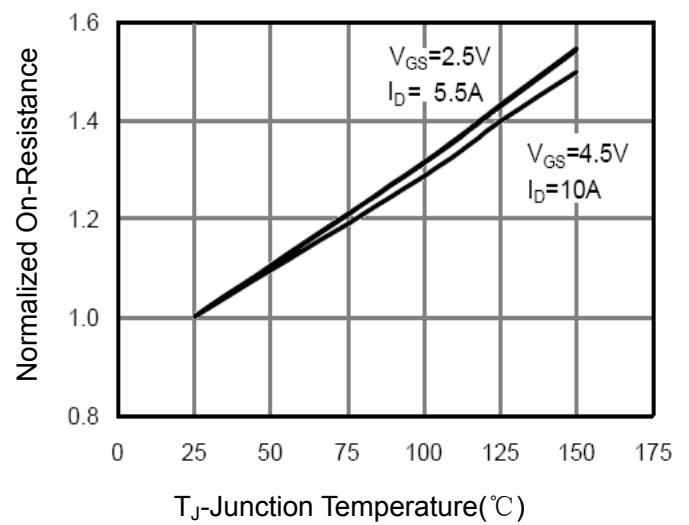
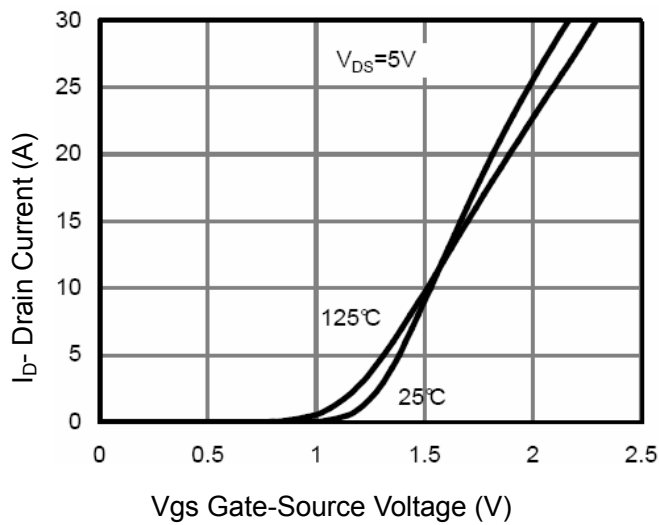


Figure 6 Drain-Source On-Resistance



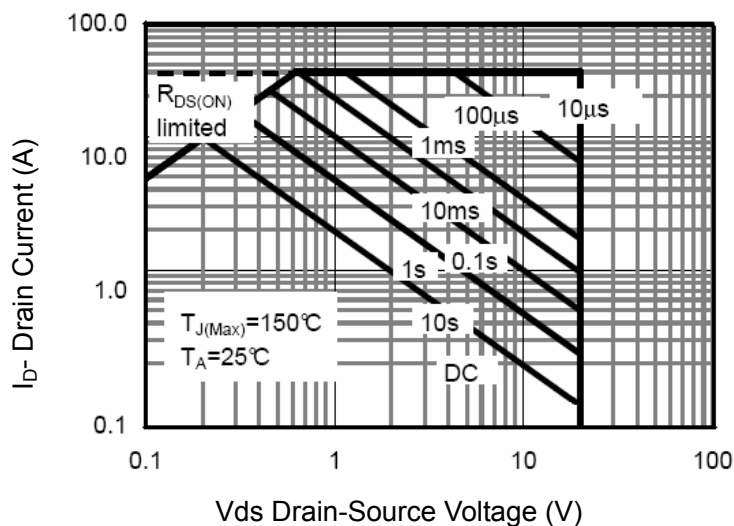


Figure 13 Safe Operation Area

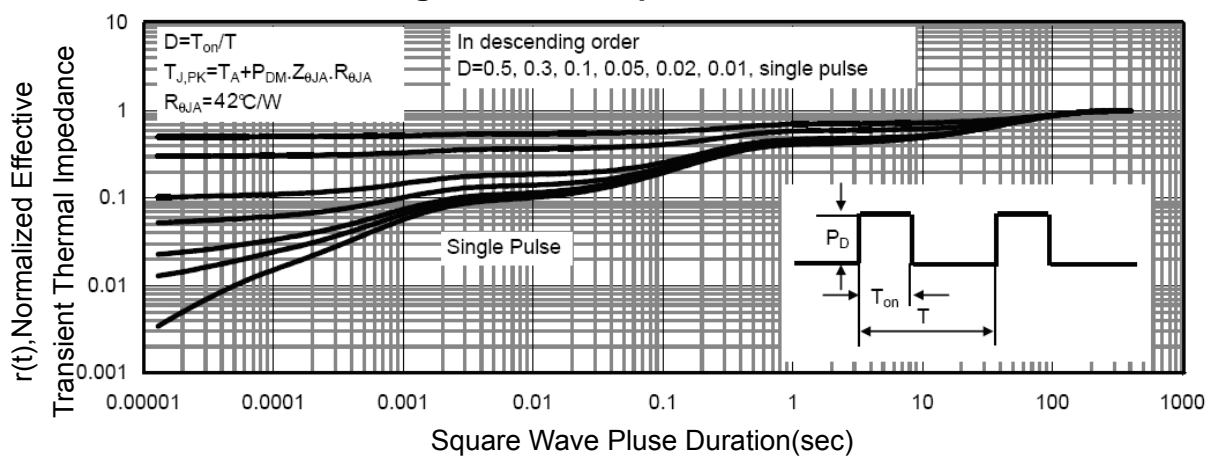
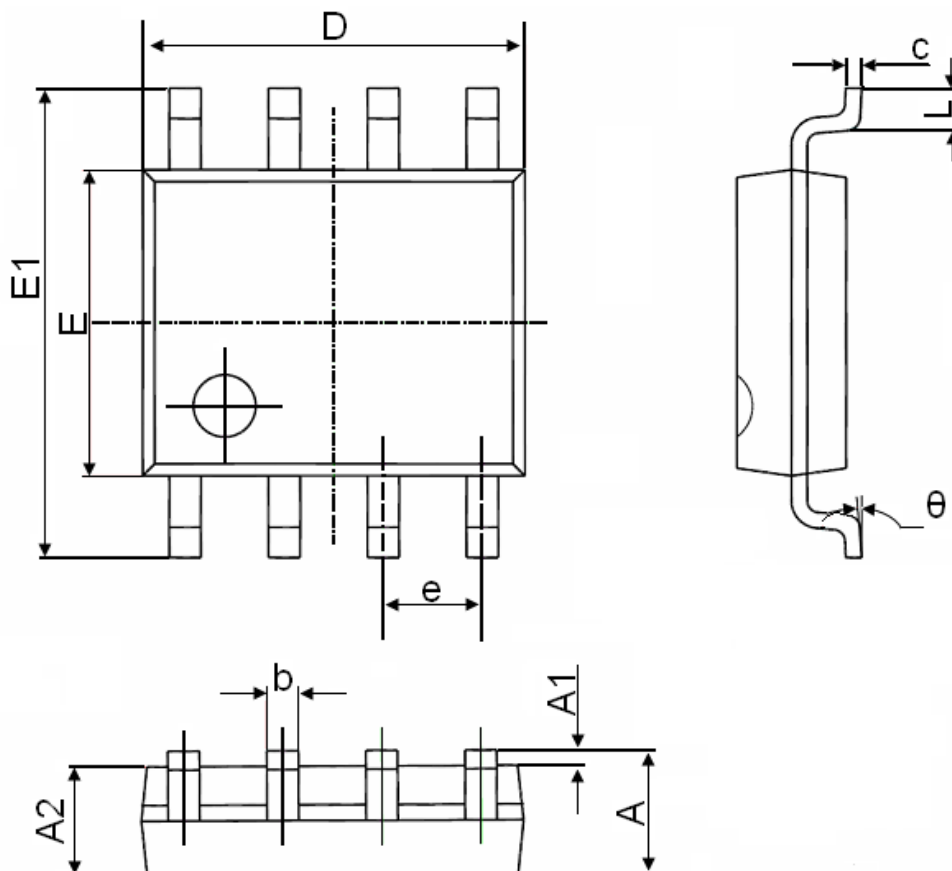


Figure 14 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°